Unigen Corp. Wireless USB Products

Part Number Family:
LETO-USB WirelessUSB™ Radio USB Devices
UGQLUE4US50A Series
Short Range Modules

Issue Date: 6 June 2007

Revision: 1.10

Revision History

Rev. No.	History	Issue Date	Remarks
0.9	Final Draft	15 Dec 2006	Update Reference Documents, Functional Description
1.0	Prelim Release	27 Dec 2006	Preliminary Release, adds EVT test data
1.1	Updated	6 Jun 2007	Updated electrical characteristics

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WirelessUSB™ - UGQLUE4US

Solutions for a Real Time World **Data Sheet**

Table of Contents:

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REFERENCE DOCUMENTATION:

The Unigen LETO-USB (UGQLUE4US50A) WirelessUSB™ USB devices of the Cypress Semiconductor CY7C64215 enCoRe III full speed USB controller and CYRF6936 LP 2.4GHz DSSS Radio SOC is represented in this document. The detail provided is information for using LETO-USB in a digital electronic device and is only a "companion" document to Cypress Semiconductors' CYWRF6936 documentation for the above noted part.

The CY7C64215 enCoRe III full speed USB controller and CYRF6936 LP 2.4GHz DSSS Radio SOC 10-meter information and technical detail LP (ex. register settings, timing, application interfaces, clocking and power management, etc.) may be obtained from the Cypress Semiconductor web site or contacting Cypress's authorized sales representatives.

The following is a list of required documents and locations known at the time of publication that accompany this datasheet.

- The CY7C64215 enCoRe III full speed USB controller Datasheet – CY7C64215.pdf http://download.cypress.com/publishedcontent/publish/design_resources/datasheets/contents/cy7c64215_8.pdf
- The CYRF6936 LP 2.4GHz DSSS Radio SOC Datasheet – CYRF6936.pdf http://download.cypress.com/publishedcontent/publish/design_resources/datasheets/contents/cyrf6936_8.pdf

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INTRODUCTION:

Unigen LETO-USB WirelessUSB™ LP 10+ meter range module represent the convergence of emerging wireless connectivity solutions and the USB "Plug-N-Play" ease of operation. WirelessUSB™, as created by Cypress Semiconductor, is a low-cost, 2.4GHz communication protocol designed for use in commercial, industrial, consumer, and computer product applications needing highly reliable data connectivity.

LETO-USB device combine Cypress Semiconductor's wireless and USB expertise with Unigen's module design, manufacturing, and testing proficiency to create production ready, pre-certified devices that are easily integrated into existing, and new product designs.

LETO-USB device offer immediate, drop-in design solutions and use the native Operating System HID drivers to seamlessly enumerate and operate mouse, keyboard, and gaming devices, or other devices using the HID specification for communication with the host systems.

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FEATURES:

- **USB 2.0 full speed**
- **Complete Transceiver Radio module: CYRF6936 LP 2.4GHz DSSS Radio SOC,** Tuned Matching RF Network, 10ppm crystal, complete PCBA including trace antenna and universal 12 position interface header
- **Operates in the 2.4 to 2.483GHz, unlicensed frequency range (ISM – Industrial, Scientific and Medical)**
- **Transmit power up to +4dBm**
- **Receive sensitivity up to -97dBm**
- **Transmission Range up to 50 meters NLOS**
- **DSSS data rates up to 250 kbps, GFSK data rate of 1 Mbps**
- **Auto Transaction Sequencer (ATS) - no MCU intervention**
- **Framing, Length, CRC16, and Auto ACK**
- **Fast Startup and Fast Channel Changes**
- **Separate 16-byte Transmit and Receive FIFOs**
- **AutoRate™ - dynamic data rate reception**
- **Receive Signal Strength Indication (RSSI)**
- **Serial Peripheral Interface (SPI) control while in sleep mode**
- **4-MHz SPI microcontroller interface**
- **Operating voltage from 3.0V to 5.25V**
- **Sleep Current <20mA**
- **Operating current 35mA-62mA at 5V,** Internal PA setting 5 (-5dBm) thru 7 (+4dBm)
- **Operating temperature from 0 to 70°C**
- **Small PCBA Design:** 1.5" x 0.66" x 0.224" (38.1mm x 16.8mm x 5.7 mm*) *board to board height
- **FCC Device Approval:** FCC Part 15, EN 300328-1, EN 301 489-1, and Industry Canada RSS-210 standards
- **No additional regulatory RF test needed for listed countries**

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DESCRIPTION:

LETO-USB WirelessUSB™ devices are tightly integrated, low-cost, high-reliability 2.4GHz TX/RX communications devices for use with Human Interface Device (HID) class compliant products.

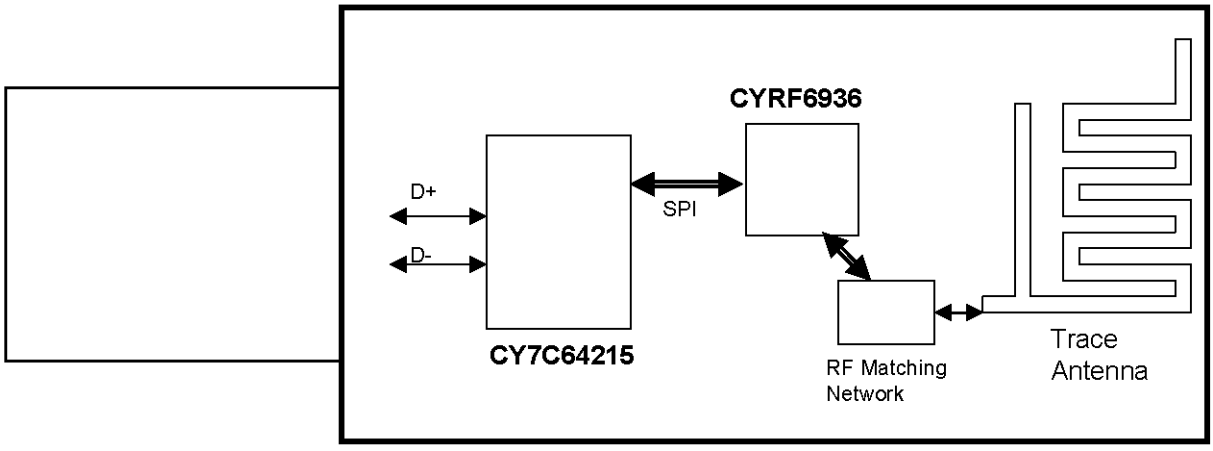
The LETO-USB devices use the Cypress Semiconductor CY7C64215 enCoRe III full speed USB controller and CYRF6936 LP 2.4GHz DSSS Radio SOC device

LETO-USB devices are a complete radio solution requiring only integration into an existing, or new device.

LETO-USB devices are 100% tested for functional operation and are pre-screened for FCC Part 15 compliance. The devices are supplied with an integrated antenna. For applications where the integrated antenna is unsuitable, model LP are available that support using an external coaxial antenna. Unigen recommends using a 2dBi gain dipole antennae for customers requiring an external antenna.

LETO-USB devices are intended for use in computer and consumer product/device applications and use the OS native HID class drivers to enable compliant devices. In most applications, *no additional host drivers are required*. The devices are suitable for use in embedded and/or industrial applications as well.

FUNCTIONAL BLOCK DIAGRAMS:



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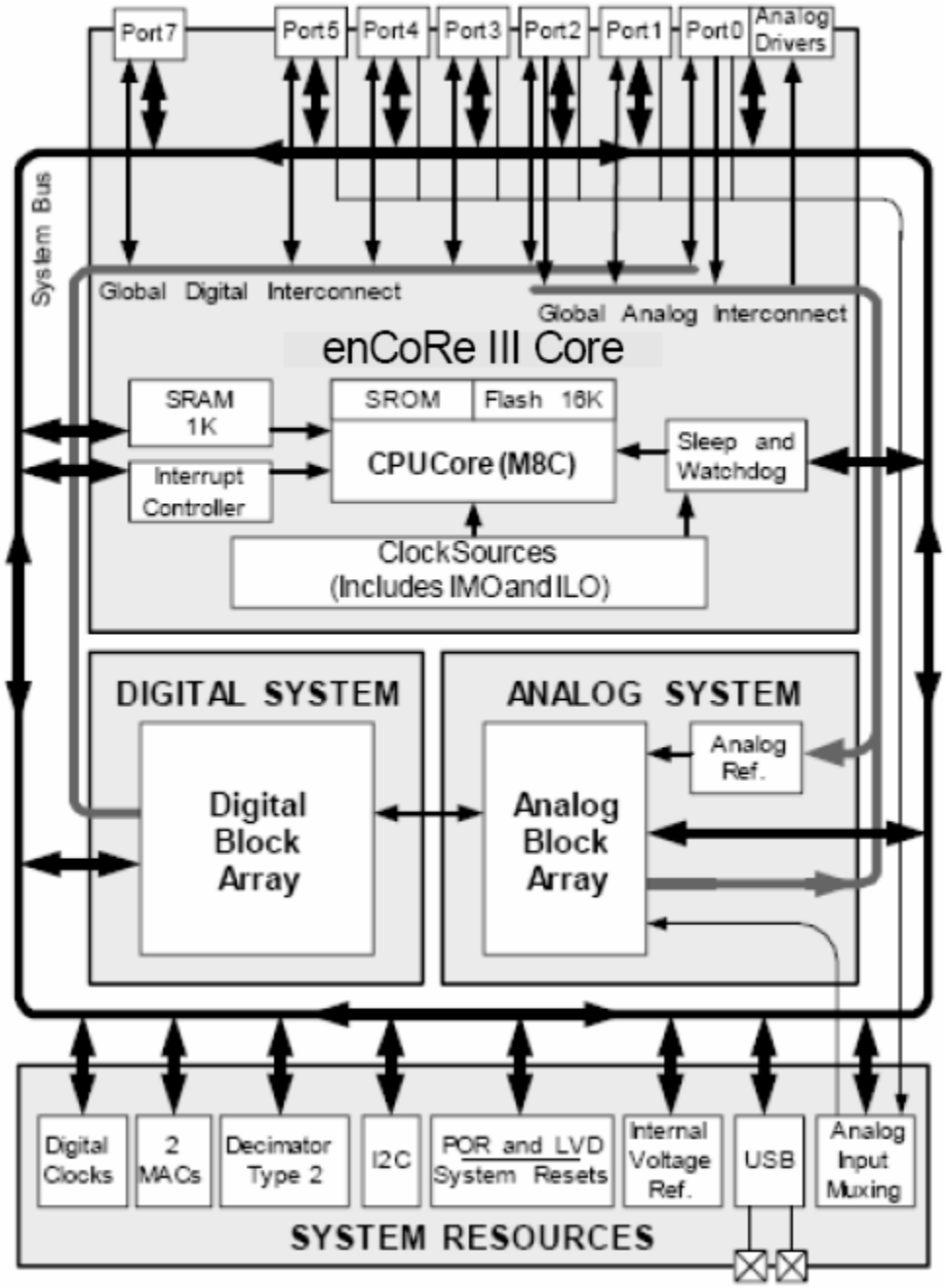
CY7C64215 Simplified Block Diagram



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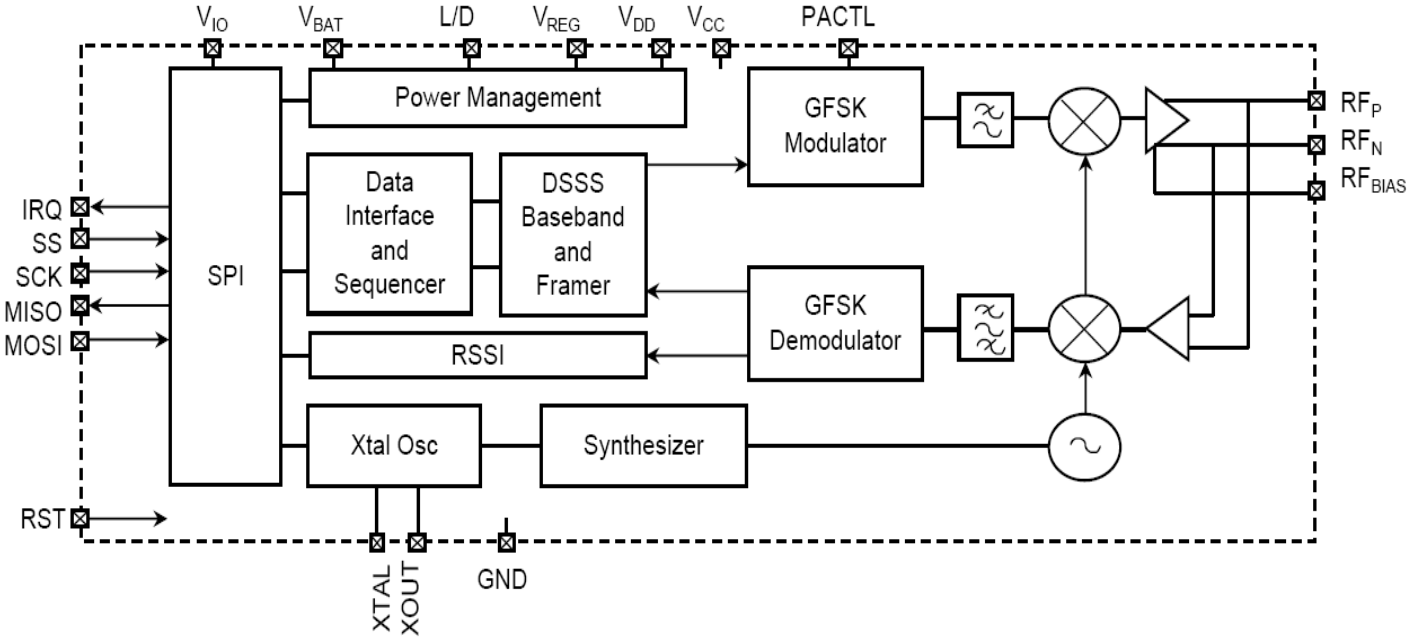
CYRF6936 Simplified Block Diagram



ABSOLUTE MAXIMUM RATINGS:

Symbol	Definition	Min.	Max.	Unit
VCC	Supply Voltage	-0.5	6.0	VDC
TS	Storage Temperature Range	-55	100	°C
TAP	Ambient Temperature with Power Applied	-40	85	°C
VLI	VDC to Logic Inputs	-0.5	VCC + 0.5	VDC
V O/Hi-Z	VDC to Outputs in High-Z state	-0.5	VCC + 0.5	VDC
SDVD	Static Discharge Voltage Digital		>2000	VDC
SDVR	Static Discharge Voltage RF		>1100	VDC
LUC	Latch-up Current	+200	-200	mA

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These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of this module. Avoid using the module outside the recommended operating conditions defined below. This module is ESD sensitive and should be handled and/or used in accordance with proper ESD mitigation.

RECOMMENDED OPERATING CONDITIONS:

Symbol	Description	Value			
		Min.	Typ.*	Max.	Unit
VCC	Supply Voltage	4.5	-	5.25	VDC
TOC	Commercial Operating Temperature Range	0	25	70	°C
GND	Ground Voltage		0		VDC

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DC ELECTRICAL CHARACTERISTICS:

Symbol	Description	Condition(s)	Value			
			Min.	Typ.*	Max.	Unit
V_{CC}	Supply Voltages		3.0	-	5.25	V
V_{OH1}	Voltage Output High Condition 1	At I_{OH} = –100.0µA	V_{CC} - 0.2	V_{CC}		V
V_{OH2}	Voltage Output High Condition 2	At I_{OH} = –2.0 mA	V_{CC} - 0.4	V_{CC}		V
V_{OL}	Voltage Output Low	At I_{OL} = 2.0 mA		0.0	0.75	V
V_{IH}	Voltage Input High		0.7 V_{CC}		V_{CC}	V
V_{IL}	Voltage Input Low		0		0.8 V_{CC}	V
I_{IL}	Input Leakage Current	0 < V_{IN} < V_{CC}	-1	0.26	+1	µA
I_{CC} (GSFK)	Average TX I_{CC}, 1Mbps, slow channel	PA=5, 2-way, 4-bytes/10 ms		0.87		mA
I_{CC} (32-8DR)	Average TX I_{CC}, 250kbps, fast channel	PA=5, 2-way, 4-bytes/10 ms		1.2		mA
I_{SB}	Sleep Mode I_{CC}	PMU disabled		20.8	22	µA
IDLE I_{CC}	Radio off, XTAL Active	XOUT disabled		21.0		mA
I_{SYNTH}	I_{CC} During Synth Start			28.4		mA
TX I_{CC}	TX I_{CC} During Transmit (V_{CC} 3.3VDC)	PA = 0 (-35 dBm)	36.1	36.4	36.7	mA
TX I_{CC}	TX I_{CC} During Transmit (V_{CC} 3.3VDC)	PA = 1 (-30 dBm)	36.4	36.7	37.0	mA
TX I_{CC}	TX I_{CC} During Transmit (V_{CC} 3.3VDC)	PA = 2 (-24 dBm)	36.9	37.2	37.5	mA
TX I_{CC}	TX I_{CC} During Transmit (V_{CC} 3.3VDC)	PA = 3 (-18 dBm)	37.3	37.6	37.9	mA
TX I_{CC}	TX I_{CC} During Transmit (V_{CC} 3.3VDC)	PA = 4 (-13 dBm)	38.1	38.4	38.7	mA
TX I_{CC}	TX I_{CC} During Transmit (V_{CC} 3.3VDC)	PA = 5 (-5 dBm)	39.8	40.1	40.4	mA
TX I_{CC}	TX I_{CC} During Transmit (V_{CC} 3.3VDC)	PA = 6 (0 dBm)	42.8	43.1	43.4	mA
TX I_{CC}	TX I_{CC} During Transmit (V_{CC} 3.3VDC)	PA = 7 (+4 dBm)	49.1	49.4	49.7	mA
RX I_{CC}	RX I_{CC} During Receive (V_{CC} 3.3VDC)	LNA off, ATT on	38.1	38.6	39.1	mA
RX I_{CC}	RX I_{CC} During Receive (V_{CC} 3.3VDC)	LNA on, ATT off	41.5	42.0	42.5	mA
MTBF		Calculated			>87,600	Hours

Table – Electrical Characteristics

*= Measured with 5.0VCC at 25ºC

[1]= Mean Icc when transmitting a 5-byte packet (3 data bytes + 2 bytes of protocol) every 10ms using the Wireless USB LP 1-way protocol.

[2]= Mean Icc when transmitting a 5-byte packet (3 data bytes + 2 bytes of protocol) every 10ms using the Wireless USB LP 2-way protocol.

Notes
5. It is permissible to connect voltages above VIO to inputs through a series resistor limiting input current to 1 mA. AC timing not guaranteed.
6. Human Body Model (HBM).
7. VREG depends on battery input voltage.
8. In sleep mode, the I/O interface voltage reference is VBAT.
10. Includes current drawn while starting crystal, starting synthesizer, transmitting packet (including SOP and CRC16), changing to receive mode, and receiving ACK handshake. Device is in sleep except during this transaction.
11. ISB is not guaranteed if any I/O pin is connected to voltages higher than VIO.

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RADIO PARAMETERS:

Parameter Description	Condition	Min.	Typ.	Max	Unit
RF Frequency Range		2.400	ISM	2.497	GHz
Radio Receiver (T = 25ºC, V_{CC} = 3.3V, f_{OSC}= 12.000000MHz, BER ≤10^{-3}					
Sensitivity 125kbps 64-8DR	BER 1E-3		-97		dBm
Sensitivity 250kbps 32-8DR	BER 1E-3		-93		dBm
Sensitivity	CER 1E-3	-80	-87		dBm
Sensitivity GFSK	BER 1E-3, ALL SLOW =1		-84		dBm
LNA Gain	LNA On		22.8		dB
ATT Gain	ATT On		-31.7		dB
Maximum Received Signal	LNA On	-15	-6		dBm
RSSI Value for PWR_{in} >-60dBm	LNA On		21		Count
RSSI Slope			1.9		dB/Count
Interference Performance (CER 1E-3)					
Co-channel Interference rejection Carrier-to-Interference (C/I)	C = –60 dBm		9		dB
Adjacent (±1 MHz) channel selectivity C/I 1 MHz	C = –60 dBm		3		dB
Adjacent (±2 MHz) channel selectivity C/I 2 MHz	C = –60 dBm		-30		dB
Adjacent (≥ 3 MHz) channel selectivity C/I > 3 MHz	C = –67 dBm		-38		dB
Out-of-band Blocking Interference Signal Frequency					
30MHz – 12.75GHz	C = –67 dBm		-30		dBm
Intermodulation	C = –64 dBm, Δf = 5, 10MHz		-36		dBm
Receive Spurious Emission					
800 MHz	100 kHz ResBW		-79		dBm
1.6 GHz	100 kHz ResBW		-71		dBm
3.2 GHz	100 kHz ResBW		-65		dBm
Radio Transmitter (T = 25ºC, Vcc = 3.3V)					
Maximum RF Transmit Power	PA = 7	+2	+4	+6	dBm
Maximum RF Transmit Power	PA = 6	-2	0	+2	dBm
Maximum RF Transmit Power	PA = 5	-7	-5	-3	dBm
Maximum RF Transmit Power	PA = 4	-15	-13	-11	dBm
Maximum RF Transmit Power	PA = 3	-20	-18	-16	dBm
Maximum RF Transmit Power	PA = 2	-26	-24	-22	dBm
Maximum RF Transmit Power	PA = 1	-32	-30	-27	dBm
Maximum RF Transmit Power	PA = 0	-37	-35	-33	dBm
RF Power Control Range			39		dB
RF Power Range Control Step Size	Seven steps, monotonic		5.6		dB
Frequency Deviation Min	PN Code Pattern 10101010		270		kHz
Frequency Deviation Max	PN Code Pattern 11110000		323		kHz
Error Vector Magnitude (FSK Error)	>0 dBm		10%		dB
Zero Crossing Error			±125		ns
Occupied Bandwidth	100 kHz ResBW, -6dBc	500	876		kHz
Initial Frequency Offset			±75		kHz
Transmission In-Band Spurious (PA = 7)					
Second Channel Power (±2 MHz)			-38		dBm
≥ Third Channel Power (≥3 MHz)			-44		dBm
Non-Harmonically Related Spurs (PA = 7)					
800 MHz			-38		dBm
1.6 GHz			-34		dBm
3.2 GHz			-47		dBm
Harmonic Spurs (PA = 7)					
Second Harmonic	4.8 GHz		-43		dBm
Third Harmonic	7.2 GHz		-48		dBm
Fourth and Greater Harmonics	>9 GHz		-59		dBm

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Power Management					
Crystal Start to 10 ppm			0.7	1.3	ms
Crystal Start to IRQ	XSIRQ EN=1		0.6		ms
Synth Settle	Slow channels			270	µs
Synth Settle	Medium channels			180	µs
Synth Settle	Fast channels			100	µs
Link turn-around time	GFSK			30	µs
Link turn-around time	250 kbps			62	µs
Link turn-around time	125kbps			94	µs
Link turn-around time	<125kbps			31	µs
Maximum Packet Length	All modes except 64 DDR			40	bytes
Maximum Packet Length	64 DDR			16	bytes

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AGENCY CERTIFICATIONS (PRE-SCAN):

Agency	Test Performed	Type	Limit	Result	Margin
EU	Radiated Spurious Emissions	30-12.75MHz Transmit Mode	EN 300 328	PASS	-4.6dB @ 4804MHz
		30-12.75MHz Transmit Mode	EN 300 328	PASS	-4.9 @ 177.01MHz
FCC 15.247	Radiated Emissions	30 25,000 Spurious Emissions	FCC Part 15.209/15.247 (c)	PASS	Results on File
		6dB Bandwidth	15.247(a)	PASS	960kHz
		99% Bandwidth	IC RSS-210	PASS	1.175MHz
		Output Power	15.247(b)	PASS	7.2dBm
		Power Spectral Density (PSD)	15.247(d)	PASS	3.06dBm
		Bandedge	FCC Part 15.209 /15.247(c)	PASS	Results on File
		Out of band	15.247(c)	PASS	Results on File
EU	Radio Performance Test	Output Power, Power spectral density at normal conditions	EN 300 328-1	PASS	Results on File
		Frequency Range at normal conditions	EN 300 328-1	PASS	Results on File
		Output Power over extreme conditions	EN 300 328-1	TBT	
		Frequency Range over extreme conditions	EN 300 328-1	TBT	
		Conducted spurious emissions, 30MHz - 12750MHz, transmit mode	EN 300 328-1	PASS	Results on File
		Conducted spurious emissions, 30MHz - 12750MHz, receive/stand-by mode	EN 300 328-1	PASS	Results on File
	Radiated Spurious Emissions	30 - 12,750 MHz -Spurious Emissions Transmit Mode	EN 300 328 V1.2.1	PASS	Results on File
		30 - 12,750 MHz -Spurious Emissions Receive Mode	EN 300 328 V1.2.1	PASS	Results on File

Table – Regulatory Agency Certifications

REGULATORY COMPLIANCE STATEMENT:

The device has been pre-scanned against the relevant requirements of standards: EN 300 328, EN 301 489-17, FCC part 15 and Industry Canada RSS-210. The device is certified by the regulatory authorities in the USA and Canada and complies with the applicable essential requirements of the Radio & Telecommunication Terminal Equipment (R&TTE) directive in the EU. The device can thus be incorporated into products sold worldwide with little or no additional testing of the module itself. ***The end product must meet the appropriate technical requirements that apply to that product type but re-certification of the radio module is not required in the USA and Canada.***

In the EU, the integrator is responsible for evaluating their product type per the essential performance requirements of the R&TTE directive (except those associated with the module), declaring compliance and then notifying the member states prior to marketing the product (because the module uses a frequency band that is not harmonized in the EU). It is the responsibility of the module integrator to obtain the necessary approval to sell products incorporating this module in other countries outside of North America and the EU. The report of measurements performed on the module in compliance with the FCC rules and EN standards can be used in these submittal (as the requirements in many other markets around the world are based in part or in whole on the standards prevalent in North America and the EU).

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FUNCTIONAL OVERVIEW:

The CY7C64215, enCoRe III is based on the flexible PSoC architecture and is a full-featured, full-speed (12 Mbps) USB part. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of consumer, and communication applications.

The CYRF6936 IC provides a complete WirelessUSB SPI to antenna wireless MODEM. The SoC is designed to implement wireless device links operating in the worldwide 2.4-GHz ISM frequency band. It is intended for systems compliant with world-wide regulations covered by ETSI EN 301 489-1 V1.41, ETSI EN 300 328-1 V1.3.1 (Europe), FCC CFR 47 Part 15 (USA and Industry Canada) and TELEC ARIB_T66_March, 2003 (Japan). The SoC contains a 2.4-GHz 1-Mbps GFSK radio transceiver, packet data buffering, packet framer, DSSS baseband controller, Received Signal Strength Indication (RSSI), and SPI interface for data transfer and device configuration. The radio supports 98 discrete 1-MHz channels (regulations may limit the use of some of these channels in certain jurisdictions). The baseband performs DSSS spreading/despreading, Start of Packet (SOP), End of Packet (EOP) detection and CRC16 generation and checking. The baseband may also be configured to automatically transmit Acknowledge (ACK) handshake packets whenever a valid packet is received. When in receive mode, with packet framing enabled, the device is always ready to receive data transmitted at any of the supported bit rates enabling the implementation of mixed-rate systems in which different devices use different data rates. This also enables the implementation of dynamic data rate systems, which use high data rates at shorter distances and/or in a low-moderate interference environment, and change to lower data rates at longer distances and/or in high interference environments. In addition, the CYRF6936 IC has a Power Management Unit (PMU) which allows direct connection of the device to any battery voltage in the range 1.8V to 3.6V. The PMU conditions the battery voltage to provide the supply voltages required by the device, and may supply external devices.

Data Transmission Modes

The SoC supports four different data transmission modes:
- In GFSK mode, data is transmitted at 1 Mbps, without any DSSS.
- In 8DR mode, 8 bits are encoded in each derived code symbol transmitted.
- In DDR mode, 2-bits are encoded in each derived code symbol transmitted. (As in the CYWUSB6934 DDR mode).
- In SDR mode, 1 bit is encoded in each derived code symbol transmitted. (As in the CYWUSB6934 standard modes.)

Both 64-chip and 32-chip Pseudo-Noise (PN) Codes are supported. The four data transmission modes apply to the data after the SOP. In particular the length, data, and CRC16 are all sent in the same mode. In general, lower data rates reduce packet error rate in any given environment.

Link Layer Modes

The CYRF6936 IC device supports the following data packet framing features:

SOP – Packets begin with a 2-symbol Start of Packet (SOP) marker. This is required in GFSK and 8DR modes, but is optional in DDR mode and is not supported in SDR mode; if framing is disabled then an SOP event is inferred whenever two successive correlations are detected. The SOP_CODE_ADR code used for the SOP is different from that used for the "body" of the packet and if desired may be a different length. SOP must be configured to be the same length on both sides of the link.

Length – There are two options for detecting the end of a packet. If SOP is enabled, then the length field should be enabled. GFSK and 8DR must enable the length field. This is the first 8-bits after the SOP symbol, and is transmitted at the payload data rate. When the length field is enabled, an End of Packet (EOP) condition is inferred after reception of the number of bytes defined in the length field, plus two bytes for the CRC16 (when enabled—see below). The alternative to using the length field is to infer an EOP condition from a configurable number of successive non-correlations; this option is not available in GFSK mode and is only recommended to enable when using SDR mode.

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CRC16 – The device may be configured to append a 16-bit CRC16 to each packet. The CRC16 uses the USB CRC polynomial with the added programmability of the seed. If enabled, the receiver will verify the calculated CRC16 for the payload data against the received value in the CRC16 field. The seed value for the CRC16 calculation is configurable, and the CRC16 transmitted may be calculated using either the loaded seed value or a zero seed; the received data CRC16 will be checked against both the configured and zero CRC16 seeds. CRC16 detects the following errors:
- Any one bit in error
- Any two bits in error (no matter how far apart, which column, and so on)
- Any odd number of bits in error (no matter where they are)
- An error burst as wide as the checksum itself

Figure 6-1 shows an example packet with SOP, CRC16 and lengths fields enabled, and *Figure 6-2* shows a standard ACK packet.

Figure 6-1. Example Packet Format

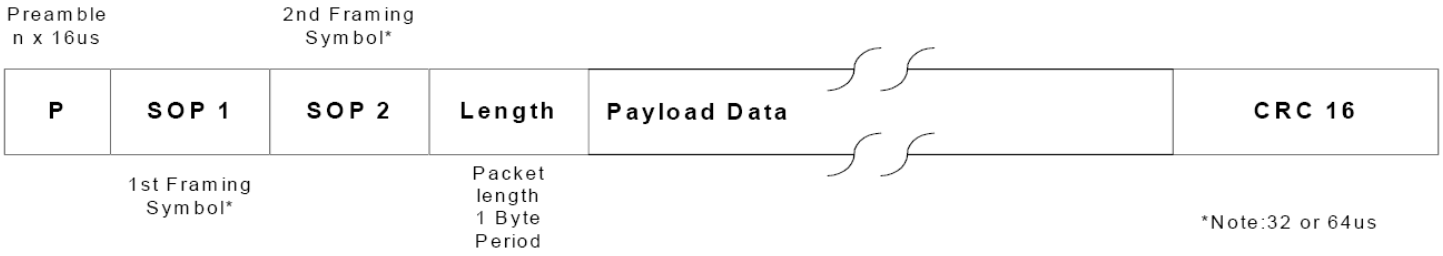
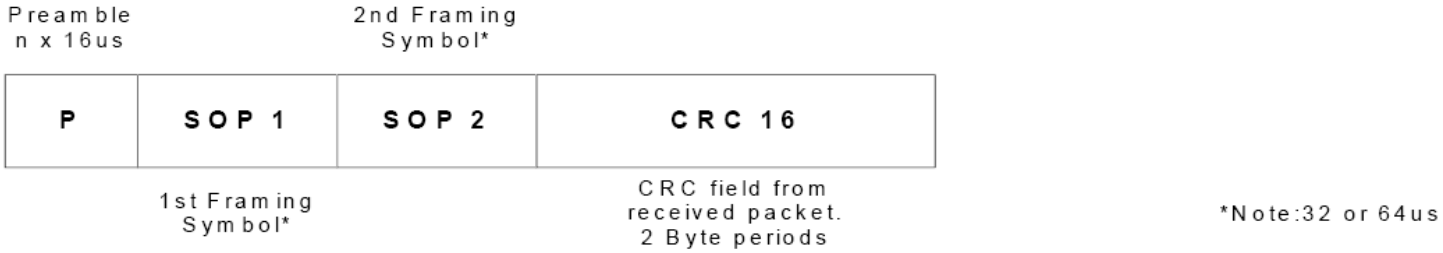


Figure 6-2. Example ACK Packet Format



Packet Buffers

All data transmission and reception utilizes the 16-byte packet buffers—one for transmission and one for reception. The transmit buffer allows a complete packet of up to 16-bytes of payload data to be loaded in one burst SPI transaction, and then transmitted with no further MCU intervention. Similarly, the receive buffer allows an entire packet of payload data up to 16 bytes to be received with no firmware intervention required until packet reception is complete. The CYRF6936 IC supports packets up to 255 bytes, however, actual maximum packet length will depend on accuracy of the clock on each end of the link and the data mode; interrupts are provided to allow an MCU to use the transmit and receive buffers as FIFOs. When transmitting a packet longer than 16 bytes, the MCU can load 16-bytes initially, and add further bytes to the transmit buffer as transmission of data creates space in the buffer. Similarly, when receiving packets longer than 16 bytes, the MCU must fetch received data from the FIFO periodically during packet reception to prevent it from overflowing.

Auto Transaction Sequencer (ATS)

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The CYRF6936 IC provides automated support for transmission and reception of acknowledged data packets. When transmitting in transaction mode, the device automatically:
• starts the crystal and synthesizer
• enters transmit mode
• transmits the packet in the transmit buffer
• transitions to receive mode and waits for an ACK packet
• transitions to the transaction end state when either an ACK packet is received, or a timeout period expires Similarly, when receiving in transaction mode, the device automatically:
• waits in receive mode for a valid packet to be received
• transitions to transmit mode, transmits an ACK packet
• transitions to the transaction end state (receive mode to await the next packet, etc.) The contents of the packet buffers are not affected by the transmission or reception of ACK packets. In each case, the entire packet transaction takes place without any need for MCU firmware action (providing packets of 16 bytes or less are used); to transmit data the MCU simply needs to load the data packet to be transmitted, set the length, and set the TX GO bit. Similarly, when receiving packets in transaction mode, firmware simply needs to retrieve the fully received packet in response to an interrupt request indicating reception of a packet.

Backward Compatibility
The CYRF6936 IC is fully interoperable with the main modes of the first generation devices. The 62.5-kbps mode is supported by selecting 32-chip DDR mode. Similarly, the 15.675-kbps mode is supported by selecting 64-chip SDR mode. In this way, a suitably configured CYRF6936 IC device may transmit data to and/or receive data from a first generation device. Disabling the SOP, length, and CRC16 fields is required for backwards compatibility.

Data Rates
By combining the PN code lengths and data transmission modes described above, the CYRF6936 IC supports the following data rates:
• 1000-kbps (GFSK)
• 250-kbps (32-chip 8DR)
• 125-kbps (64-chip 8DR)
• 62.5-kbps (32-chip DDR)
• 31.25-kbps (64-chip DDR)
• 15.625-kbps (64-chip SDR)

Functional Block Overview

2.4-GHz Radio
The radio transceiver is a dual conversion low IF architecture optimized for power and range/robustness. The radio employs channel-matched filters to achieve high performance in the presence of interference. An integrated Power Amplifier (PA) provides up to +4 dBm transmit power, with an output power control range of 34 dB in 7 steps. The supply current of the device is reduced as the RF output power is reduced.

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Internal PA Output Power Step Table

PA Setting	Typical Output Power (dBm)
7	+4
6	0
5	-5
4	-13
3	-18
2	-24
1	-30
0	-35

Typical Range Observed Table

Environment	Typical Range (meters)
LOS	50
NLOS	30
Home/Office	20
Note: Range observed PA=7, Fremont, CA	

Frequency Synthesizer

Before transmission or reception may commence, it is necessary for the frequency synthesizer to settle. The settling time varies depending on channel; 25 fast channels are provided with a maximum settling time of 100-µs. The "fast channels" (<100-µs settling time) are every 3rd channel, starting at 0 up to and including 72 (i.e., 0,3,6,9…….69 & 72).

Baseband and Framer

The baseband and framer blocks provide the DSSS encoding and decoding, SOP generation and reception and CRC16 generation and checking, as well as EOP detection and length field.

Packet Buffers and Radio Configuration Registers

Packet data and configuration registers are accessed through the SPI interface. All configuration registers are directly addressed through the address field in the SPI packet (as in the CYWUSB6934). Configuration registers are provided to allow configuration of DSSS PN codes, data rate, operating mode, interrupt masks, interrupt status, etc.

SPI Interface

The CYRF6936 IC has a SPI interface supporting communications between an application MCU and one or more slave devices (including the CYRF6936). The SPI interface supports single-byte and multi-byte serial transfers using either 4-pin or 3-pin interfacing. The SPI communications interface consists of Slave Select (SS), Serial Clock (SCK), and Master Out-Slave In (MOSI), Master In-Slave Out (MISO), or Serial Data (SDAT). The SPI communications is as follows:

- Command Direction (bit 7) = "1" enables SPI write transaction. A "0" enables SPI read transactions.
- Command Increment (bit 6) = "1" enables SPI auto address increment. When set, the address field automatically increments at the end of each data byte in a burst access, otherwise the same address is accessed.
- Six bits of address.
- Eight bits of data.

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The device receives SCK from an application MCU on the SCK pin. Data from the application MCU is shifted in on the MOSI pin. Data to the application MCU is shifted out on the MISO pin. The active-low Slave Select (SS) pin must be asserted to initiate an SPI transfer.

The application MCU can initiate SPI data transfers via a multibyte transaction. The first byte is the Command/Address byte, and the following bytes are the data bytes as shown in *Figure 7-1* through *Figure 7-4*.

The SPI communications interface has a burst mechanism, where the first byte can be followed by as many data bytes as desired. A burst transaction is terminated by deasserting the slave select (SS = 1).

The SPI communications interface single read and burst read sequences are shown in *Figure 7-2* and *Figure 7-3*, respectively.

The SPI communications interface single write and burst write sequences are shown in *Figure 7-4* and *Figure 7-5*, respectively.

This interface may optionally be operated in a 3-pin mode with the MISO and MOSI functions combined in a single bidirectional data pin (SDAT). When using 3-pin mode, user firmware should ensure that the MOSI pin on the MCU is in a high impedance state except when MOSI is actively transmitting data.

The device registers may be written to or read from 1 byte at a time, or several sequential register locations may be written/read in a single SPI transaction using incrementing burst mode. In addition to single byte configuration registers, the device includes register files; register files are FIFOs written to and read from using non-incrementing burst SPI transactions.

The IRQ pin function may optionally be multiplexed onto the MOSI pin; when this option is enabled the IRQ function is not available while the SS pin is low. When using this configuration, user firmware should ensure that the MOSI pin on the MCU is in a high impedance state whenever the SS pin is high.

The SPI interface is not dependent on the internal 12-MHz clock, and registers may therefore be read from or written to while the device is in sleep mode, and the 12-MHz oscillator disabled.

The SPI interface and the IRQ and RST pins have a separate voltage reference pin (VIO), enabling the device to interface directly to MCUs operating at voltages below the CYRF6936 IC supply voltage.

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Figure - SPI Transaction Format

	Byte 1			Byte 1+N
Bit #	7	6	[5:0]	[7:0]
Bit Name	DIR	INC	Address	Data

Figure - SPI Single Read Sequence

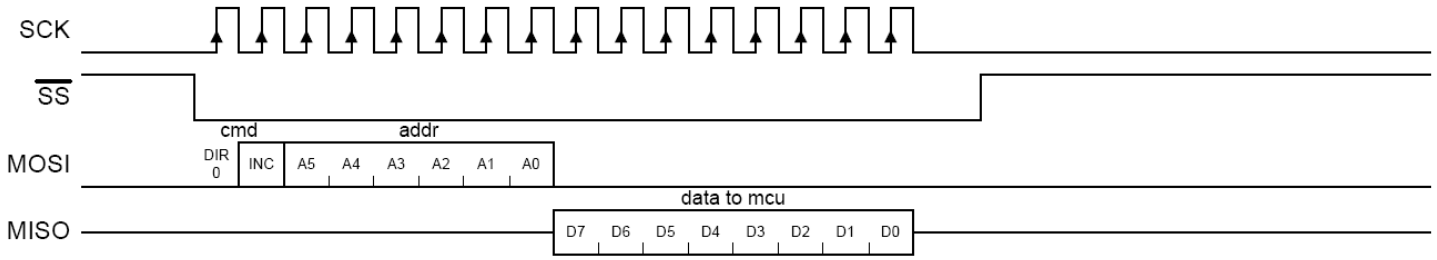

Figure - SPI Incrementing Burst Read Sequence

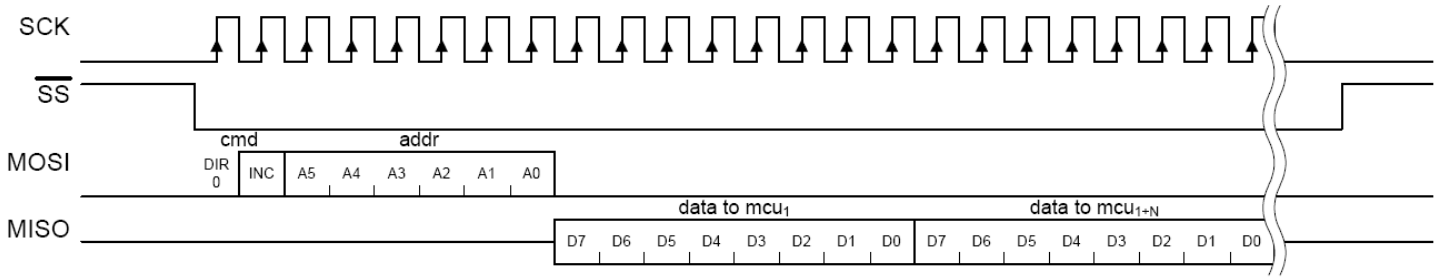

Figure - SPI Single Write Sequence

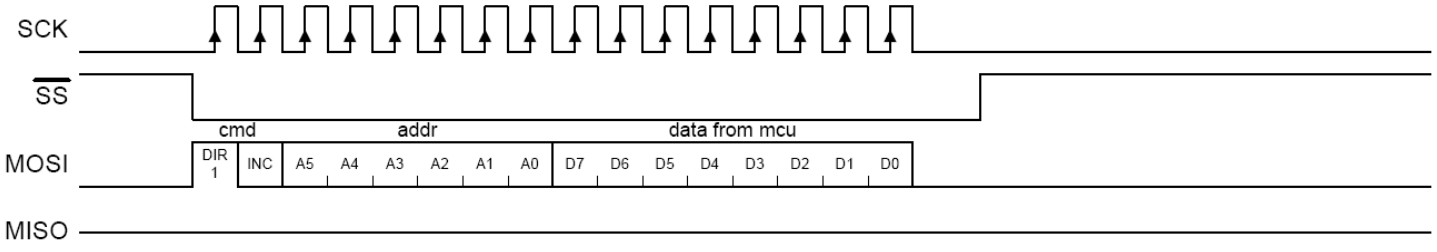

Figure - SPI Incrementing Burst Write Sequence

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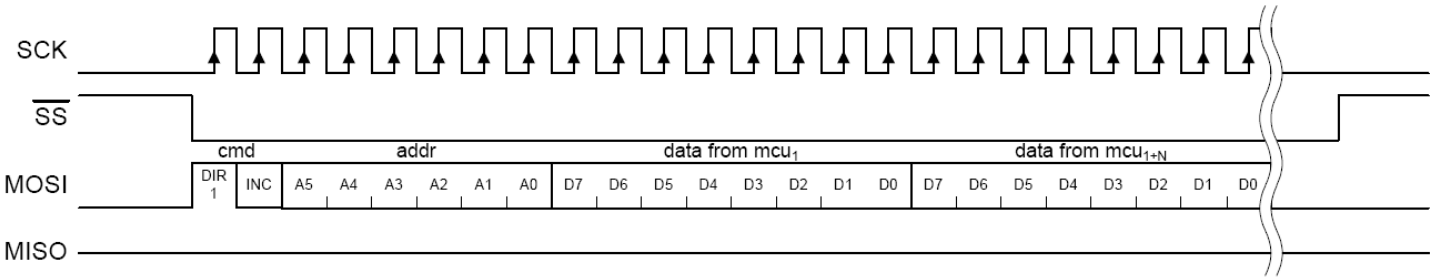

Interrupts

The device provides an interrupt (IRQ) output, which is configurable to indicate the occurrence of various different events. The IRQ pin may be programmed to be either active high or active low, and be either a CMOS or open drain output. A full description of all the available interrupts can be found in *Section 9.0*. The CYRF6936 IC features three sets of interrupts: transmit, receive, and system interrupts. These interrupts all share a single pin (IRQ), but can be independently enabled/disabled. The contents of the enable registers are preserved when switching between transmit and receive modes. If more than one interrupt is enabled at any time, it is necessary to read the relevant status register to determine which event caused the IRQ pin to assert. Even when a given interrupt source is disabled, the status of the condition that would otherwise cause an interrupt can be determined by reading the appropriate status register. It is therefore possible to use the devices without making use of the IRQ pin by polling the status register(s) to wait for an event, rather than using the IRQ pin.

Clocks

A 12-MHz crystal (30-ppm or better) is directly connected between XTAL and GND without the need for external capacitors. A digital clock out function is provided, with selectable output frequencies of 0.75-, 1.5-, 3-, 6-, or 12-MHz. This output may be used to clock an external microcontroller (MCU) or ASIC. This output is enabled by default, but may be disabled. Below are the requirements for the crystal to be directly connected to XTAL pin and GND:

Low Noise Amplifier (LNA) and Received Signal Strength Indication (RSSI)

The gain of the receiver may be controlled directly by clearing the AGC EN bit and writing to the Low Noise Amplifier (LNA) bit of the RX_CFG_ADR register. When the LNA bit is cleared, the receiver gain is reduced by approximately 20 dB, allowing accurate reception of very strong received signals (for example when operating a receiver very close to the transmitter). Approximately 30 dB of receiver attenuation can be added by setting the Attenuation (ATT) bit; this allows data reception to be limited to devices at very short ranges. Disabling AGC and enabling LNA is recommended unless receiving from a device using external PA. When the device is in receive mode the RSSI_ADR register returns the relative signal strength of the on-channel signal power. When receiving, the device will automatically measure and store the relative strength of the signal being received as a 5-bit value. An RSSI reading is taken automatically when the SOP is detected. In addition, a new RSSI reading is taken every time the previous reading is read from the RSSI_ADR register, allowing the background RF energy level on any given channel to be easily measured when RSSI is read when no signal is being received. A new reading can occur as fast as once every 12 µs.

Register Descriptions

All registers are read and writable, except where noted. Registers may be written to or read from either individually or in sequential groups.

Register Map Summary

Address	Mnemonic	b7	b6	b5	b4	b3	b2	b1	b0	Default[1]	Access[1]
0x00	CHANNEL_ADR	Not Used				Channel				-1001000	-bbbbbbb

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0x01	TX_LENGTH_ADR				TX Length					00000000	bbbbbbbb
0x02	TX_CTRL_ADR	TX GO	TX CLR	TXB15 IRQEN	TXB8 IRQEN	TXB0 IRQEN	TXBERR IRQEN	TXC IRQEN	TXE IRQEN	00000011	bbbbbbbb
0x03	TX_CFG_ADR	Not Used	Not Used	DATA CODE LENGTH	DATA MODE		PA SETTING			-000101	-bbbbbb
0x04	TX_IRQ_STATUS_ADR	OS IRQ	LV IRQ	TXB15 IRQ	TXB8 IRQ	TXB0 IRQ	TXBERR IRQ	TXC IRQ	TXE IRQEN	----------	rrrrrrrrr
0x05	RX_CTRL_ADR	RX GO	RSVD	RXB16 IRQEN	RXB8 IRQEN	RXB1 IRQEN	RXBERR IRQEN	RXC IRQEN	RXE IRQEN	00000111	-bbbbbb
0x06	RX_CFG_ADR	AGC EN	LNA	ATT	HILO	FAST TURN EN	Not Used	RXOW EN	VLD EN	10010-10	bbbbb-bb
0x07	RX_IRQ_STATUS_ADR	RXOW IRQ	SOPDET IRQ	RXB16 IRQ	RXB8 IRQ	RXB1 IRQ	RXBERR IRQ	RXC IRQ	RXE IRQ	----------	brrrrrrrr
0x08	RX_STATUS_ADR	RX ACK	PKT ERR	EOP ERR	CRC0	Bad CRC	RX Code	RX Data Mode		----------	rrrrrrrrr
0x09	RX_COUNT_ADR			RX Count						00000000	rrrrrrrr
0x0A	RX_LENGTH_ADR			RX LENGTH						00000000	rrrrrrrr
0x0B	PWR_CTRL_ADR	PMU EN	LVIRQ EN	PMU SEN	Not Used	LVI TH			PMU OUTV	10100000	bbb-bbbb
0x0C	XTAL_CTRL_ADR	XOUT FN		XSIRQ EN	Not Used	Not Used	FREQ			000—100	Bbb--bbb
0x0D	IO_CFG_ADR	IRQ OD	IRQ POL	MISO OD	XOUT OD	PACTL OD	PACTL GPIO	SPI 3PIN	IRQ GPIO	00000000	bbbbbbbb
0x0E	GPIO_CTRL_ADR	XOUT OP	MISO OP	PACTL OP	IRQ OP	XOUT IP	MISO IP	PACTL IP	IRQ IP	0000----	bbbbrrrr
0x0F	XACT_CFG_ADR	ACK EN	Not Used	FRC END			END STATE	ACK TO		1-000000	bbbbbbbb
0x10	FRAMING_CFG_ADR	SOP EN	SOP LEN	LEN EN			SOP TH			10100101	bbbbbbbb
0x11	DATA32_THOLD_ADR	Not Used	Not Used	Not Used	Not Used			TH32		----0100	----bbbb
0x12	DATA64_THOLD_ADR	Not Used	Not Used	Not Used				TH64		---01010	---bbbbb
0x13	RSSI_ADR	SOP	Not Used	LNA			RSSI			0-100000	bbbbbbbb
0x14	EOP_CTRL_ADR	HEN		HINT			EOP			10100100	bbbbbbbb
0x15	CRC_SEED_LSB_ADR	CRD SEED LSB					CRC SEED LSB			00000000	bbbbbbbb
0x16	CRC_SEED_MSB_ADR	CRC SEED MSB					CRC SEED MSB			00000000	bbbbbbbb
0x17	TX_CRC_LSB_ADR	CRC LSB					CRC LSB			--------	rrrrrrrr
0x18	TX_CRC_MSB_ADR	CRC MSB					CRC MSB			--------	rrrrrrrr
0x19	RX_CRC_LSB_ADR	CRC LSB				CRC LSB				11111111	rrrrrrrr
0x1A	RX_CRC_MSB_ADR	CRC MSB				CRC MSB				11111111	bbbbbbbb
0x1B	TX_OFFSET_LSB_ADR	STRIM LSB				STRIM LSB				0000000	bbbbbbbb
0x1C	TX_OFFSET_MSB_ADR	Not Used	Not Used	Not Used	Not Used			STRIM MSB		----0000	----bbbb
0x1D	MODE_OVERRIDE_ADR	RSVD	RSVD	FRC SEN	FRC AWAKE		Not Used	Not Used	RST	00000—0	wwwww--w
0x1E	RX_OVERRIDE_ADR	ACK RX	RXTX DLY	MAN RXACK	FRC RXDR	DIS CRC0	DIS RXCRC	ACE	Not Used	000000-	bbbbbbb-
0x1F	TX_OVERRIDE_ADR	ACK TX	FRC PRE	RSVD	MAN TXACK	OVRD ACK	DIS TXCRC	RSVD	TX INV	00000000	bbbbbbbb
0x26	XTAL_CFG_ADR	RSVD	RSVD	RSVD	RSVD	START DLY	RSVD	RSVD	RSVD	00000000	wwwwwwww
0x27	CLK_OVERRIDE_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD	00000000	wwwwwwww
0x28	CLK_EN_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD	00000000	wwwwwwww

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0x29	RX_ABORT_ADR	RSVD	RSVD	ABORT EN	RSVD	RSVD	RSVD	RSVD	RSVD	00000000	wwwwwwww
0x32	AUTO_CAL_TIME_ADR						AUTO_CAL-TIME			00000011	wwwwwwww
0x35	AUTO_CAL_OFFSET_ADR						AUTO_CAL_OFFSET			00000000	wwwwwwww
0x39	ANALOG_CTRL_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RX INV	ALL SLOW	00000000	wwwwwwww
Register Files											
0x20	TX_BUFFER_ADR	TX Buffer File					TX Buffer File			--------	wwwwwwww
0x21	RX_BUFFER_ADR	RX Buffer File					RX Buffer File			--------	rrrrrrrr
0x22	SOP_CODE_ADR	SOP Code File					SOP Code File			Note 2	bbbbbbbb
0x23	DATA_CODE_ADR	Data Code File					Data Code File			Note 3	bbbbbbbb
0x24	PREAMBLE_ADR	Preamble File					Preamble File			Note 4	bbbbbbbb
0x25	MFG_ID_ADR	MFG ID File					MFG ID File			NA	rrrrrrrr

Notes
1. b = read/write, r = read only, w = write only, - = not used, default value is undefined.
2. SOP_CODE_ADR default = 0x17FF9E213690C782.
3. DATA_CODE_ADR default = 0x02F9939702FA5CE3012BF1DB0132BE6F.
4. PREAMBLE_ADR default = 0x333302.

Mnemonic	**CHANNEL_ADR**			**Address**				**0x00**
Bit	7	6	5	4	3	2	1	0
	-		1	0	1	0	0	0
	-		R/W	R/W	R/W	R/W	R/W	RW
Function	Not Used	Channel						

Bit 7 Not Used.

Bits 6:0 This field selects the channel. 0x00 sets 2400 MHz; sets 2498 MHz. Values above 0x62 are not valid. The default channel is a fast channel above the frequency typically used in non-overlapping WiFi systems. Any write to this register will impact the time it takes the synthesizer to settle.

fast (100-us) – 0 3 6 9 12 15 18 21 24 27 30 33 36 39 42 45 48 51 54 57 60 63 66 69 72 96
medium (180-us) – 2 4 8 10 14 16 20 22 26 28 32 34 38 40 44 46 50 52 56 58 62 64 68 70 74 76 78 80 82 84 86 88 90 92 94
slow (270-us) – 1 5 7 11 13 17 19 23 25 29 31 35 35 37 41 43 47 49 53 55 59 61 65 67 71 73 75 77 79 81 83 85 87 89 91 93 95 97
Usable channels subject to regulation

Mnemonic	**TX_LENGTH_ADR**			**Address**				**0x01**
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TX Length							

Bits 7:0 This register sets the length of the packet to be transmitted. A length of zero is valid, and will transmit a packet with SOP, length CRC and CRC16 fields (if enabled), but no data field. Packet lengths of more than 16 bytes will require that some data bytes be written after transmission of the packet has begun. Typically, length is updated prior to setting TX GO. The maximum packet length for all packets is 40 bytes except for framed 64-chip DDR where the maximum packet length is 16 bytes.

Maximum packet length is limited by the delta between the transmitter and receiver crystals of 60-ppm or better.

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Mnemonic	TX_CTRL_ADR			Address				0x02
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TX GO	TX CLR		TXB8 IRQEN	TXB0 IRQEN	TXBERR IRQEN	TXC IRQEN	TXE IRQEN

Bit 7 Start Transmission. Setting this bit triggers the transmission of a packet. Writing a 0 to this flag has no effect. This bit is cleared automatically at the end of packet transmission. The transmit buffer may be loaded either before or after setting this bit. If data is loaded after setting this bit, the length of time available to load the buffer depends on the starting state (sleep, idle or synth), the length of the SOP code, the length of preamble, and the packet data rate. For example, if starting from idle mode on a fast channel in 8DR mode with 32 chip SOP codes the time abailable is 100 us (synth start) + 32 us (preamble) + 64 us (SOP length) + 32 us (length byte0 = 228 us. If there are no bytes in the TX buffer at the end of transmission of the length field, a TXBERR IRQ will occur and transmission will abort.

Bit 6 Clear TX Buffer. Writing a 1 to this register clears the transmit buffer. Writing a 0 to this bit has no effect. The previous packet (16 or fewer bytes) may be retransmitted by setting TX GO and not setting this bit. If a new transmit packet is to be loaded before/after the the TX GO bit has been set, then this bit should be set before loading a new transmit packet to the buffer.

Bit 5 Buffer Not Full Interupt Enable. See TX_IRQ_STATUS_ADR for description.

Bit 4 Buffer Half Empty Interrupt Enable. See TX_IRQ_STATUS_ADR for description.

Bit 3 Buffer Empty Interrupt Enable. See TX_IRQ_STATUS_ADR for description.

Bit 2 Buffer Error Interrupt Enable. See TX_IRQ_STATUS_ADR for description.

Bit 1 Transmission Complete Interrupt Enable. TXC IRQEN and TXE IRQEN must be set together. See TX_IRQ_STATUS_ADR for description.

Bit 0 Transmit Error Interrupt Enable. TXC IRQEN and TXE IRQEN must be set together. See TX_IRQ_STATUS_ADR for description.

Mnemonic	TX_CFG_ADR			Address				0x03
Bit	7	6	5	4	3	2	1	0
Default	-	-	0	0	1	1	0	1
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	RW
Function	Not Used	Not Used	Data Code Length	Data Mode		PA Setting		

Bit 5 Data Code Length. This bit selects the length of the DATA_CODE_ADR code for the data portion of the packet. This bit is ignored when The data mode is set to GFSK. 1= 64 chip codes. O = 32 chip codes.

Bits 4:3 Data Mode. This field sets the data transmission mode. Oo = 1-Mbps GFSK. 01 = 8DR Mode. 10= DDR Mode. 11= SDR Mode. It is recommended that firmware sets the ALL SLOW bit in register ANALOG_CTRL_ADR when using GFSK data rate mode.

Bits 2:0 PA Setting. This field sets the transmit signal strength. 0 = -30 dBm, 1 = -25 dBm, 2 = -20 dBm, 3 = dBm, 1 = -25 dBm, 2 = -20 dBm, 3 = -15dBm, 4 = -10 dBm, 5 = -5 dBm, 6 = 0 dBm, 7 = +4 dBm.

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Mnemonic	TX_IRQ_STATUS_ADR			Address				0x04
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	-	-	-	-
Read/Write	R	R	R	R	R	R	R	R
Function	OS IRQ	LV IRQ	TXB15 IRQ	TXB8 IRQ	TXB0 IRQ	TXVERR IRQ	TXC IRQ	TXE IRQ

The state of all IRQ status bits is valid regardless of whether or not the IRQ is enabled. The IRQ output of the device is in its active state whenever one or more bits in this register is set and the corresponding IRQ enable bit is also set. Status bits are non-atomic (different flags may change value at different times in response to a single event).

Bit 7 Osciliator Stable IRQ Status. This bit is set when the internal crystal oscillator has settled (synthesizer sequence starts).

Bit 6 Low Voltage Interrupt Status. This bit is set when the voltage on VBAT is below the LVI threshold (see PWR_CTL_ADR). This interrupt is automatically disabled whenever the PMU is disabled. When enabled, this bit reflects the voltage on VBAT.

Bit 5 Buffer Not Full Interrupt Status. This bit is set whenever there are 15 or fewer bytes remaining in the the transmit buffer.

Bit 4 Buffer Half Empty Interrupt Status. This bit is set whenever there are 8 fewer bytes remaining in the transmit buffer.

Bit 3 Buffer Empty Interrupt Status. This bit is set at any time that the transmit buffer is empty.

Bit 2 Buffer Error Interrupt Status. The IRQ is triggered by either of two events: (1) When the transmit buffer (TX_BUFFER_ADR) is empty and the number of bytes remaining to be transmitted is greater than zero. (2) When a byte is written to the transmit buffer and the buffer is already full. This IRQ is cleared by setting bit TX CLE in TX_CTRL_ADR.

Bit 1 Transmission Complete Interrupt Status. This IRQ is triggered when transmission is complete. If transaction mode is not enabled then This interrupt is triggered immediately after transmission of the last bit of the CRC16. If transaction mode is enabled, this interrupt is Triggered at the end of a transaction. Reading this register clears this bit. TXC IRQ and TXE IRQ flags may change value at different times in response to a single event. If transaction mode is enabled and the first read of this register returns TXC IRQ=1 and TXE IRQ=1 and TXE IRQ=0 then firmware must execute a second read to this register to determine if an error occurred by examining the status of TXE. There can be a case when this bit is not triggered when ACK EN = 1 and there is an error in transmission. If the first read of this register returns TXC IRQ = 1 and TXE IRQ = 1 then the firmware must not execute a second read to this register for a given transaction. If an ACK is received RXC IRQ and RXE IRQ may be asserted instead of TXC IRQ and TXE IRQ.

Bit 0 Transmit Error Interrupt Status. This IRQ is triggered when there is an error in transmission. This interrupt is only applicable to transaction mode. It is triggered whenever no valid ACK packet is received within the ACK timeout period. Reading this register clears this bit. See TXC IRQ, above.

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Mnemonic	RX_CTRL_ADR			Address				0x05
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RW
Function	RX GO	RSVD	RXB16 IRQENl	RXB8 IRQEN	RXB1 IRQEN	RXBERR IRQEN	RXC IRQEN	RXE IRQEN

Bit 7 Start Receive. Setting this bit causes the device to transition to receive mode. If necessary, the crystal oscillator and synthesizer will start automatically ater this bit is set. Firmware must never clear this bit. This bit must not be set again until after it self clears. The recommended method to exit receive mode when an error has occurred is to force END STATE and then dummy read all RX_COUNT_ADR bytes from RX_BUFFER_ADR or poll RSSI_ADR.SOP (bit 7) until set. See XACT_CFG_ADR and RX_ABORT_ADR for description.

Bit 6 Reserved. Must be zero.

Bit 5 Buffer Full Interrupt Enable. See RX_IRQ_STATUS for description.

Bit 4 Buffer Half Empty Interrupt Enable. See RX_IRQ_STATUS_ADR for description.

Bit 3 Buffer Not Empty Interrupt Enable. RXB1 IRQEN must not be set when RXB8 IRQEN is set and vice versa. See RX_IRQ_STATUS_ADR for description.

Bit 2 Buffer Error Interrupt Enable. See RX_IRQ_STATUS_ADR for description.

Bit 1 Packet Reception Complete Interrupt Enable. See RX_IRQ_STATUS_ADR for description.

Bit 0 Receive Error Interrupt Enable. See RX_IRQ_STATUS_ADR for description.

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Mnemonic	RX_CFG_ADR			Address				0x06
Bit	7	6	5	4	3	2	1	0
Default	1	0	0	1	0	-	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	-	R/W	RW
Function	AGC EN	LNA	ATT	HILO	FAST TURN EN	Not Used	RXOW EN	VLD EN

Status bits are non-atomic (different flags may change value at different times in response to a single event).

Bit 7 Automatic Gain Control (AGC) Enable. When this bit is set, AGC is enabled, and the LNA is controlled by the AGC circuit. When this bit is cleared the LNA is controlled manually using LNA bit. Typical applications will clear this bit during initializination. It is recommended that this bit be cleared and bit 6 (LNA) be set unless the device will be used in a system where it may receive data from a device using an external PA to transmit signals at >+4 dBm.

Bit 6 Low Noise Amplifier (LNA) Manual Control. When AGC EN (Bit 7) is cleared, this bit controls the state of the receiver LNA; when AGC EN Is set, this bit has no effect. Setting this bit enables the LNA; clearing this bit disables the LNA. Device current in receive mode is slightly Lower when the LNA is disabled. Typical applications will set this bit during initialization.

Bit 5 Receive Attenuator Enable. Setting this bit enables the receiver attenuator. The receiver attenuator may be used to de-sensi-tize the receiver so that only very strong signals may be received. This bit should only be set when the AGC EN is disabled and the LNA is manually disabled.

Bit 4 HILO. When FAST TURN EN is set, this bit is used to select whether the device will use the high frequency for the channel selected, or The low frequency. 1 = hi; 0 = lo. When FAST TURN EN is not enabled this also controls the highlow bit to the receiver and should be Left at the default value of 1 for high side receive injection. Typical applications will clear this bit during initialization.

Bit 3 Fast Turn Mode Enable. When this bit is set, the HILO bit determines whether the device receives data transmitted 1 MHz above the RX Synthesizer frequency or 1 MHz below the receiver synthesizer frequency. Use of this mode allows for very fast turn-around, because the same synthesizer frequency may be used for both transmit and receive, thus eliminating the synthesizer resetting period between transmit and receive. Note that when this bit is set, and the HILO bit is cleared, received data bits are automatically inverted to compensate for the inversion of data received on the "image" frequency. Typical applications will set this bit during initialization.

Bit 1 Overwrite Enable. When this bit is set, if an SOP is detected while the receive buffer is not empty, then the existing contents of receive Buffer are lost, and the new packet is loaded into the receive buffer. When this bit is set, the RXOW IRQ is enabled. If this bit is cleared, Then the receive buffer may not be over-written by a new packet, and whenever the receive buffer is not empty SOP conditions are Ignored, and it is not possible to receive data until the previously received packet has been completely read from the receive buffer.

Bit 0 Valid Flag Enable. When this bit is set, the receive buffer can store up to 8 bytes of data interleaved with valids (data0, valids0, data1, valids1…). Typically, this bit is set only when interoperability with first generation devices is desired. See RX_BUFFER_ADR for more detail.

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Mnemonic	RX_IRQ_STATUS_ADR			Address				0x07
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	-	-	-	-
Read/Write	R/W	R	R	R	R	R	R	R
Function	RXOW IRQ	SOPDET IRQ	RXB16 IRQ	RXB8 IRQ	RXB1 IRQ	RXBERRIRQ	RXC IRQ	RXE IRQ

The state of all IRQ Status bits is valid regardless of whether or not the IRQ is enabled. The IRQ output of the device is in its active state whenever one or more bits in this register is set and the corresponding IRQ enable bit is also set. Status bits are non-atomic (different flags may change value at different times in response to a single event). In particular, standard error handling is only effective if the premature termination of a transmission due to an exception does not leave the device in an inconsistent state.

Bit 7 Receive Overwrite Interrupt Status. This IRQ is triggered when the receive buffer is over-written by a packet being received before the previous packet has been read from the buffer. This bit is cleared by writing any value to this register. This condition is only possible when the RXOWEN bit in RX_CFG_ADR is set. This bit must be written "1" by firmware before the new packet may be read from the receive buffer.

Bit 6 Start of packet detect. This bit is set whenever the start of packet symbol is detected.

Bit 5 Receiver Buffer Full Interrupt Status. This bit is set whevever the receive buffer is full, and cleared otherwise.

Bit 4 Receive Buffer Half Full Interrupt Status. This bit is set whenever there are 8 or more bytes remaining in the receive buffer. Firmware must Read exactly eight bytes when reading RXB8 IRQ.

Bit 3 Receive Buffer Not Empty Interrupt Status. This bit is set at any time that there are 1 or more bytes in the receive buffer, and cleared when the receive buffer is empty. It is possible, in rare cases, that the last byte of a packet may remain in the buffer even though the RXB1 IRQ flag has cleared. This can ONLY happen on the last byte of a packet and only if the packet data is being read out of the buffer while the packet is still being received. The flag is trustworthy under all other conditions, and for all bytes prior to the last. When using RXB1 IRQ and unloading the packet data during reception, the user should be sure to check the RX_COUNT_ADR value after the RXC IRQ/RXE IRQ is set and unload the last remaining bytes if the number of bytes unloaded is less than the reported count, eventhough the RXB1 IRQ is not set.

Bit 2 Receive Buffer Error Interrupt Status. This IRQ is triggered in one of two ways: (1) When the receive buffer is empty and there is an attempt to read data. (2) When the receive buffer is full and more data is received. This flag is cleared when RX GO is set and a SOP is received.

Bit 1 Packet Receive Complete Interrupt Status. This IRQ is triggered when a packet has been received. If transaction mode is enabled, then this bit is not set until after transmission of the ACK. If transaction mode is not enabled then this bit is set as soon as a valid packet is received. This bit is cleared when this register is read. RXC IRQ and RXE IRQ flags may change value at different times response to a single event. There are cases when this bit is not triggered when ACK EN = 1 and there is an error in reception. Therefore, firmware should examine RXC IRQ, RXE IRQ, and CRC 0 to determine receive status. If the first read of this register returns RXC IRQ = 1 and RXE IRQ = 0 then firmware must execute a second read to this register to determine if an error occurred by examining the status of RXE IRQ. If the first read of this register returns RXC IRQ = 1 and RXE IRQ = 1 then the firmware must not execute a second read to this register for a given transaction.

Bit 0 Receive Error Interrupt Status. This IRQ is triggered when there is an error in reception. It is triggered whenever a packet is received with a bad CRC16, an unexpected EOP is detected, a packet type (data or ACK) mismatch, or a packet is dropped because the receive buffer is still not empty when the next packet starts. The exact cause of the error may be determined by reading RX_STATUS_ADR. This bit is cleared when this register is read.

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Mnemonic	RX_STATUS_ADR			Address				0x08
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	-	-	-	-
Read/Write	R	R	R	R	R	R	R	R
Function	RX ACK	PKT ERR	EOP ERR	CRC0	Bad CRC	RX Code	RX Data Mode	

It is expected that firmware does not read this register until after TX GO self clears. Status bits are non-atomic (different flags may change value at different times in response to a single event)

Bit 7 RX Packet Type. This bit is set when the received packet is an ACK packet, and cleared when the received packet is a standard packet.

Bit 6 Receive Packet Type Error. This bit is set when the packet type received is what not was expected and cleared when the packet type received was as expected. For example, if data packet is expected and an ACK is received, this bit will be set.

Bit 5 Unexpected EOP. This bit is set when an EOP is detected before the expected data length and CRC 16 fields have been received. This bit is cleared when SOP pattern for the next packet has been received. This includes the case where there are invalid bits detected in the length field and the length field is forced to 0.

Bit 4 Zero-seed CRC 16. This bit is set whenever the CRC 16 of the last received packet has a zero seed.

Bit 3 Bad CRC 16. This bit is set when the CRC 16 of the last received packet is incorrect.

Bit 2 Receive Code Length. This bit indicated the DATA_CODE_ADR code length used in the last correctly received packet. 1 = 64-chip code, 0 = 32-chip code.

Bit 1:0 Receive Data Mode. These bits indicate the data mode of the last correctly received packet. 00 = 1-Mbps GFSK 01 = 8DR 10 = DDR. 11 = Not Valed. These bits do not apply to unframed packets.

Mnemonic	RX_COUNT_ADR			Address				0x09
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Function	RX Count							

Count bits are non-atomic (updated at different times).

Bits 7:0 This register contains the total number of payload bytes received during reception of the current packet. After packet reception is complete, this register will match the value in RX_LENGTH_ADR unless there was a packet error. This register is cleared when RX_LENGTH_ADR is automatically loaded, if length is enabled, after the SOP. Count should not be read when RX_GO=1 during a transaction.

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Mnemonic	RX_LENGTH_ADR			Address				0x0A
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Function	RX Length							

Lengths bits are non-atomic (different flags may change value at different times in response to a single event).

Bits 7:0 This register contains the length field which is updated with the reception of a new length field (shortly after start of packet detected). If there is an error in the received length field, 0x00 is loaded instead, except when using GFSK datarate, and an error is flagged.

Mnemonic	PWR_CTRL_ADR			Address				0x0B
Bit	7	6	5	4	3	2	1	0
Default	1	0	1	-	0	0	0	0
Read/Write	R/W	R/W	R/W	-	R/W	R/W	R/W	RW
Function	PMU EN	LVIRQ EN	PMU SEN	Not Used	LVI TH		PMU OUTV	

Bit 7 Power Management Unit (PMU) Enable. Setting this bit enables the PMU. When the PMU is disabled, or if the PMU is enabled and the VBAT voltage is above the value set in Bits 1:0 of this register, the VREG pin is internally connected to the VBAT pin. If the PMU is enabled and VBAT voltage is below the value set by PMU OUTV, then the PMU will boost the VREG pin to a voltage not less than the value set by PMU OUTV.

Bit 6 Low Voltage Interrupt Enable. Setting this bit enables the LV IRQ interrupt. When this interrupt is enabled, if the VBAT voltage falls below the threshold set by LVI TH, then a low voltage interrupt will be generated. The LVI is not available when the device is in sleep mode. The LVI event on IRQ pin is automatically disabled whenever the PMU is disabled.

Bit 5 PMU Sleep Mode Enable. If this bit is set, the PMU will continue to operate normally when the device is in sleep mode. If this bit is not set, Then the PMU is disabled when the device is in sleep mode. In this case, if VBAT is below the PMU OUTV voltage and PMU EN is set, when The device enters sleep mode the VREG voltage falls to the VBAT voltage as the VBAT voltage as the VREG capacitors discharge.

Bits 3:2 Low Voltage Interrupt Threshold. This field sets the voltage VBAT at which the LVI is triggered. 11 = 1.8V; 10 = 2.0V; 01 = 2.2v; 00 = PMU OUTV voltage.

Bits 1:0 PMU Output Voltage. This field sets the minimum output voltage of the PMU. 11 = 2.4V; 10 = 2.5V; 01 = 2.6V; 00 = 2.7V. When the PMU Is active, the voltage output by the PMU on VREG will never be less than this voltage provided that the total load on the VREG pin is less Than the specified maximum value, and the voltage in VBAT is greater than the specified minimum value.

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Mnemonic	XTAL_CTRL_ADR			Address				0x0C
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	1	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	XOUT FN		XSIRQ EN	Not Used	Not Used	FREQ		

Bits 7:6 XOUT Pin Function. This field selects between the different functions of the XOUT pin. 00 = Clock frequency set by XOUT FREQ: 01 = Active LOW PA Control: 10 = Radio data serial bit stream. If this option is selected and SPI is configured for 3-wire mode then the MISO pin will output a serial clock associated with this data stream: 11 = GPIO. To disable this output, set to GPIO mode, and set the GPIO state in IO_CFG_ADR.

Bit 5 Crystal Stable Interrupt Enable. This bit enables the OS IRQ interrupt. When enabled, this interrupt generates an IRQ event when the crystal has stabilized after the device has woken from sleep mode. This event is cleared by writing zero to this bit.

Bits 2:0 XOUT Frequency. This field sets the frequency output on the XOUT pin when XOUT FN is set to 00. 0 = 12 MHz; 1 = 6 MHz, 2 = 3MHz, 3 = 1.5 MHz, 4 = 0.75 MHz; other values are not defined.

Mnemonic	IO_CFG_ADR			Address				0x0D
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	IRQ OD	IRQ POL	MISO OD	XOUT OD	PACTL OD	PACTL GPIO	SPI 3PIN	IRQ GPIO
Function	Not Used	Channel						

To use a GPIO pin as an input, the output mode must be set to open drain, and a "1" written to the corresponding output register bit.

Bit 7 IRQ Pin Drive Strength. Setting this bit configures the IRQ pin as an open drain output. Clearing this bit configures the IRQ pin as a standard CMOS output, with the output "1" drive voltage being equal to the VIO pin voltage.

Bit 6 IRQ Polarity. Setting this bit configures the IRQ signal polarity to be active HIGH. Clearing this bit configures the IRQ signal polarity to be active low.

Bit 5 MISO Pin Drive Strength. Setting this bit configures the MISO pin as an open drain output. Clearing this bit configures the MISO pin as a standard CMOS output, with the output "1" drive voltage being equal to the VIO pin voltage.

Bit 4 XOUT Pin Drive Strength. Setting this bit configures the XOUT pin as an open drain output. Clearing this bit configures the XOUT pin as a standard CMOS output, with the output "1" drive voltage being equal to the VIO pin voltage.

Bit 3 PACTL Pin Drive Strength. Setting this bit configures the PACTL pin as an open drain output. Clearing this bit configures the PACTL pin as a standard CMOS output, with the output "1" drive voltage being equal to the VIO pin voltage.

Bit 2 PACTL Pin Function. When this bit is set the PACTL pin is available for use as a GPIO.

Bit 1 SPI Mode. When this bit is cleared, the SPI interface acts as a standard 4-wire SPI Slave interface. When this bit is set, the SPI interface operates in "3-Wire Mode" combining MISO and MOSI on the same pin (SDAT), and the MISO pin is available as a GPIO pin.

Bit 0 IRQ Pin Function. When this bit is cleared, the IRQ pin is asserted when an IRQ is active; the polarity of this IRQ signal is configurable In IRQ POL. When this bit is set, the IRQ pin is available for use as a GPIO pin, and the IRQ function is multiplexed onto the MOSI pin. In this case the IRQ signal state is presented on the MOSI pin whenever the SS signal is inactive (HIGH). Usable channels subject to regulation

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Mnemonic	GPIO_CTRL_ADR			Address				0x0E
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	-	-	-	-
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	XOUT OP	MISO OP	PACTL OP	IRQ OP	XOUT IP	MISO IP	PACTL IP	IRQ IP

To use a GPIO pin as an input, the output mode must be set to open drain, and a "1" written to the corresponding output register bit.

Bit 7 XOUT Output. When the XOUT pin is configured to be a GPIO, the state of this bit sets the output state of the XOUT pin.

Bit 6 MISO Output. When the MISO pin is configured to be a GPIO, the state of this bit sets the output state of the MISO pin.

Bit 5 PACTL Output. When the PACTL pin is configured to be a GPIO, the state of this bit sets the output state of the PACTL pin.

Bit 4 IRQ Output. When the IRQ pin is configured to be a GPIO, the state of this bit sets the output state of the IRQ pin.

Bit 3 XOUT Input. The state of this bit reflects the voltage on the XOUT pin.

Bit 2 MISO Input. The state of this bit reflects the voltage on the MISO pin.

Bit 1 PACTL Input. The state of this bit reflects the voltage on the PACTL pin.

Bit 0 IRQ Input. The state of this bit reflects the voltage on the IRQ pin.

Mnemonic	XACT_CFG_ADR			Address				0x0F
Bit	7	6	5	4	3	2	1	0
Default	-		1	0	1	0	0	0
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Function	ACK EN	Not Used	FRC END	END STATE			ACK TO	

Bit 7 Acknowledge Enable. When this bit is set, an ACK packet is automatically transmitted whenever a valid packet is received; in this case the device is considered to be in transaction mode. After transmission of the ACK packet, the device automatically transitions to the END STATE. When this bit is cleared, the device transitions directly to the END STATE immediately after the end of packet transmission. This bit affects both transmitting and receiving devices.

Bit 5 Force End State. Setting this bit forces a transition to the state set in END STATE. By setting the desired END STATE at the same time as setting this bit the device may be forced to immediately transition from its current state to any other state. This bit is automatically cleared upon completion. Firmware MUST never try to force END STATE while TX GO is set, nor when RX GO is set and a SOP has already been received (packet reception already in progress).

Bits 4:2 Transaction End State. This field defines the mode to which the device transitions after receiving or transmitting a packet. 000 = Sleep Mode; 001 = Idle Mode; 010 = Synth Mode (TX); 011 = Synth Mode (RX); 100 = RX Mode. In normal use, this field will typically be set to 000 or 001 when the device is transmitting packets, and 100 when the device is receiving packets. Note that when the device transitions to receive mode as an END STATE, the receiver must still be armed by setting RX GO before the device can begin receiving data. If the system only support packets <=16 bytes then firmware should examine RXC IRQ and RXE IRQ to determine the status of the packet. If the system supports packets > 16 bytes ensure that END STATE is not sleep, force RXF=1, perform receive operation, force RXF=0, and if necessary set END STATE back to sleep.

Bits 1:0 ACK Timeout. When the device is configured for transaction mode, this field sets the timeout period after transmission of a packet during which an ACK must be correctly received in order to prevent a transmit error condition from being detected. This

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timeout period is expressed in terms of a number of SOP_CODE_ADR code lengths; if SOP LEN is set, then the timeout period is this value multiplied by 64 μs and if SOP LEN is cleared then the timeout is this value multiplied by 32 μs. 00 = 4x; 01 = 8x, 10 = 12x; 11 = 15x the SOP_CODE_ADR code length. ACK_TO must be set to greater than 30 + Data Code Length (only for 8DR) + Preamble Length + SOP Code Length (x2).

Mnemonic	FRAMING_CFG_ADR			Address				0x10
Bit	7	6	5	4	3	2	1	0
Default	1	0	1	0	0	1	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RW
Function	SOP EN	SOP LEN	LEN EN	SOP TH				

Bit 7 SOP Enable. When this bit is set, each transmitted packet begins with a SOP field, and only packets beginning with a valid SOP field will be received. If this bit is cleared, no SOP field will be generated when a packet is transmitted, and packet reception will begin whenever two successive correlations against the DATA_CODE_ADR code are detected.

Bit 6 SOP PN Code Length. When this bit is set the SOP_CODE_ADR code length is 64 chips. When this bit is cleared the SOP_CODE_ADR code length is 32 chips.

Bit 5 Packet Length Enable. When this bit is set the 8-bit value contained in TX_LENGTH_ADR is transmitted immediately after the SOP field. In receive mode, the 8 bits immediately following the SOP field are interpreted as the length of the packet. When this bit is cleared no packet length field is transmitted. 8DR always sends the packet length field (LEN EN setting is ignored). GFSK requires user set LEN EN = 1.

Bits 4:0 SOP Correlator Threshold. This is the receive data correlator threshold used when attempting to detect a SOP symbol. There is a single threshold for the SOP_CODE_ADR code. This threshold is applied independently to each of SOP1 and SOP2 fields. When SOP LEN is set, all 5 bits of this field are used. When SOP LEN is cleared, the most significant bit is disregarded. Typical applications configure SOP TH = 04h for SOP32 and SOP TH = 0Eh for SOP64.

Mnemonic	DATA32_THOLD_ADR			Address				0x11
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	0	1	0	0
Read/Write	-	-	-	-	R/W	R/W	R/W	R/W
Function	Not Used	Not Used	Not Used	Not Used	TH32			

Bits 7:4 Not Used.

Bits 3:0 32 Chip Data PN Code Correlator Threshold. This register sets the correlator threshold used in DSSS modes when DATA CODE LENGTH (see TX_CFG_ADR) is set to 32. Typical applications configure TH32 = 05h.

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Mnemonic	DATA64_THOLD_ADR			Address				0x12
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	0	1	0	0
Read/Write	-	-	-	R/W	R/W	R/W	R/W	R/W
Function	Not Used	Not Used	Not Used	TH64				

Bits 7:4 Not Used.

Bits 3:0 64 Chip Data PN Code Correlator Threshold. This register sets the correlator threshold used in DSSS modes when DATA CODE LENGTH (see TX_CFG_ADR) is set to 64. Typical applications configure TH64 = 0Eh.

Mnemonic	RSSI_ADR			Address				0x13
Bit	7	6	5	4	3	2	1	0
Default	0	-	1	0	0	0	0	0
Read/Write	R	-	R	R	R	R	R	R
Function	SOP	Not Used	LNA	RSSI				

A Received Signal Strength Indicator (RSSI) reading is taken automatically when an SOP symbol is detected. In addition, an RSSI reading is taken whenever RSSI_ADR is read. The contents of this register are not valid after the device is configured for receive mode until either a SOP symbol is detected, or the register is (re)read. The conversion can occur as often as once every 12-µs. The approximate slope of the curve is 1.9 dB/count, but is not guaranteed.

If it is desired to measure the background RF signal strength on a channel before a packet has been received then the MCU should perform a “dummy” read of this register, the results of which should be discarded. This “dummy” read will cause an RSSI measurement to be taken, and therefore subsequent readings of the register will yield valid data.

Bit 7 SOP RSSI Reading. When set, this bit indicates that the reading in the RSSI field was taken when a SOP symbol was detected. When cleared, this bit indicates that the reading stored in the RSSI field was triggered by a previous SPI read of this register.

Bit 5 LNA State. This bit indicates the LNA state when the RSSI reading was taken. When cleared, this bit indicates that the LNA was disabled when the RSSI reading was taken; if set this bit indicates that the LNA was enabled when the RSSI reading was taken.

Bits 4:0 RSSI Reading. This field indicates the instantaneous strength of the RF signal being received at the time that the RSSI reading was taken. A larger value indicates a stronger signal. The signal strength measured is for the RF signal on the configured channel, and is measured after the LNA stage.

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Mnemonic	EOP_CTRL_ADR			Address				0x14
Bit	7	6	5	4	3	2	1	0
Default	1	0	1	0	0	1	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	HEN	HINT		EOP				

If the LEN EN bit is set, then the contents of this register have no effect. If the LEN EN bit is cleared, then this register is used to configure how an EOP (end of packet) condition is detected.

Bit 7 EOP Hint Enable. When set, this bit will cause an EOP to be detected if no correlations have been detected for the number of symbol periods set by the HINT field and the last two received bytes match the calculated CRC16 for all previously received bytes. Use of this mode reduces the chance of non-correlations in the middle of a packet from being detected as an EOP condition.

Bits 6:4 EOP Hint Symbol Count. The minimum number of symbols of consecutive non-correlations at which the last two bytes are checked against the calculated CRC16 to detect an EOP condition.

Bits 4:0 EOP Symbol Count. An EOP condition is deemed to exist when the number of consecutive non-correlations is detected.

Mnemonic	CRC_SEED_LSB_ADR			Address				0x15
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CRC SEED LSB							

The CRC16 seed allows different devices to generate or recognize different CRC16s for the same payload data. If a transmitter and receiver use a randomly selected CRC16 seed, the probability of correctly receiving data intended for a different receiver is 1/65535, even if the other transmitter/receiver are using the same SOP_CODE_ADR codes and channel.

Bits 7:0 CRC16 Seed Least Significant Byte. The LSB of the starting value of the CRC16 calculation.

Mnemonic	CRC_SEED_MSB_ADR			Address				0x16
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CRC SEED MSB							

Bits 7:0 CRC16 Seed Most Significant Byte. The MSB of the starting value of the CRC16 calculation.

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Mnemonic	TX_CRC_LSB_ADR			Address				0x17
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	-	-	-	-
Read/Write	R	R	R	R	R	R	R	R
Function	TX CRC LSB							
Bits 7:0	Calculated CRC16 LSB. The LSB of the CRC16 that was calculated for the last transmitted packet. This value is only valid after packet transmission is complete.							

Mnemonic	TX_CRC_MSB_ADR			Address				0x18
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	-	-	-	-
Read/Write	R	R	R	R	R	R	R	R
Function	TX CRC MSB							
Bits 7:0	Calculated CRC16 MSB. The MSB of the CRC16 that was calculated for the last transmitted packet. This value is only valid after packet transmission is complete.							

Mnemonic	RX_CRC_LSB_ADR			Address				0x19
Bit	7	6	5	4	3	2	1	0
Default	1	1	1	1	1	1	1	1
Read/Write	R	R	R	R	R	R	R	R
Function	RX CRC LSB							
Bits 7:0	Received CRC16 LSB. The LSB of the CRC16 field extracted from the last received packet. This value is valid whether or not The CRC16 field matched the calculated CRC16 of the received packet.							

Mnemonic	RX_CRC_MSB_ADR			Address				0x1A
Bit	7	6	5	4	3	2	1	0
Default	1	1	1	1	1	1	1	1
Read/Write	R	R	R	R	R	R	R	R
Function	RX CRC MSB							
Bits 7:0	Received CRC16 MSB. The MSB of the CRC16 field extracted from the last received packet. This value is valid whether or not The CRC16 field matched the calculated CRC16 of the received packet.							

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Mnemonic	TX_OFFSET_LSB_ADR			Address				0x1B
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R	R	R	R	R	R	R
Function	STRIM LSB							

Bits 7:0 The least significant 8 bits of the synthesizer offset value. This is a 12-bit 2's complement signed number which may be used to offset the transmit frequency of the device by up to ±1.5 MHz. A positive value increases the transmit frequency, and a negative value reduces the transmit frequency. A value of +1 increases the transmit frequency by 732.6 Hz; a value of –1 decreases the transmit frequency by 732.6 Hz. A value of 0x0555 increases the transmit frequency by 1 MHz; a value of 0xAAB decreases the transmit frequency by 1 MHz. Typically, this register is loaded with 0x55 during initialization. Typically this feature is used to avoid the need to change the synthesizer frequency when switching between TX and RX. As the IF = 1 MHz the RX frequency is offset 1 MHz from the synthesizer frequency; therefore, transmitting with a 1 MHz offset allows the same synthesizer frequency to be used for both transmit and receive.

Synthesizer offset has no effect on receive frequency.

Mnemonic	TX_OFFSET_MSB_ADR			Address				0x1C
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	0	0	0	0
Read/Write	-	-	-	-	R/W	R/W	R/W	R/W
Function	Not Used	Not Used	Not Used	Not Used	STRIM MSB			

Bits 7:4 Not Used

Bits 3:0 The most significant 4 bits of the synthesizer trim value. Typically, this register is loaded with 0x05 during initialization.

Mnemonic	MODE_OVERRIDE_ADR			Address				0x1D
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	-	-	0
Read/Write	W	W	W	W	W	-	-	W
Function	RSVD	RSVD	FRC SEN	FRC AWAKE		Not Used	Not Used	RST

Bits 7:6 Reserved. Must be zero.

Bit 5 Manually Initiate Synthesizer. Setting this bit forces the synthesizer to start. Clearing this bit has no effect. For this bit to operate correctly, the oscillator must be running before this bit is set.

Bits 4:3 Force Awake. Force the device out of sleep mode. Setting both bits of this field forces the oscillator to keep running at all times regardless of the END STATE setting. Clearing both of these bits disables this function.

Bits 2:1 Not Used.

Bit 0 Reset. Setting this bit forces a full reset of the device. Clearing this bit has no effect.

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Mnemonic	RX_OVERRIDE_ADR			Address				0x1E
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	-
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Function	ACK RX	RXTX DLY	MAN RXACK	FRC RXDR	DIS CRC0	DIS RXCRC	ACE	Not Used

This register provides the ability to over-ride some automatic features of the device.

Bit 7 When this bit is set, the device uses the transmit synthesizer frequency rather than the receive synthesizer frequency for the given channel when automatically entering receive mode.

Bit 6 When this bit is set and ACK EN is enabled, the transmission of the ACK packet is delayed by 20 μs.

Bit 5 Force Expected Packet Type. When this bit is set, and the device is in receive mode, the device is configured to receive an ACK packet at the data rate defined in TX_CFG_ADR.

Bit 4 Force Receive Data Rate. When this bit is set, the receiver will ignore the data rate encoded in the SOP symbol, and will receive data at the data rate defined in TX_CFG_ADR.

Bit 3 Reject packets with a zero-seed CRC16. Setting this bit causes the receiver to reject packets with a zero-seed, and accept only packets with a CRC16 that matches the seed in CRC_SEED_LSB_ADR and CRC_SEED_MSB_ADR.

Bit 2 The RX CRC16 checker is disabled. If packets with CRC16 enabled are received, the CRC16 will be treated as payload data and stored in the receive buffer.

Bit 1 Accept Bad CRC16. Setting this bit causes the receiver to accept packets with a CRC16 that do not match the seed in CRC_SEED_LSB_ADR and CRC_SEED_MSB_ADR. An ACK is to be sent regardless of the condition of the received CRC16.

Bit 0 Not Used.

Mnemonic	TX_OVERRIDE_ADR			Address				0x1F
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	ACK TX	FRC PRE	RSVD	MAN TXACK	OVRD ACK	DIS TXCRC	RSVD	TX INV

This register provides the ability to over-ride some automatic features of the device.

Bit 7 When this bit is set, the device uses the receive synthesizer frequency rather than the transmit synthesizer frequency for the given channel when automatically entering transmit mode.

Bit 6 Force Preamble. When this bit is set, the device will transmit a continuous repetition of the preamble pattern (see PREAMBLE_ADR) after TX GO is set. This mode is useful for some regulatory approval procedures. Firmware should set bit RST of MODE_OVERRIDE_ADR to exit this mode.

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Bit 5 Reserved. Must be zero.

Bit 4 Transmit ACK Packet. When this bit is set, the device sends an ACK packet when TX GO is set.

Bit 3 ACK Override. Use TX_CFG_ADR to determine the data rate and the CRC16 used when transmitting an ACK packet.

Bit 2 Disable Transmit CRC16. When set, no CRC16 field is present at the end of transmitted packets.

Bit 1 Reserved. Must be zero.

Bit 0 TX Data Invert. When this bit is set the transmit bitstream is inverted.

Mnemonic	XTAL_CFG_ADR			Address				0x26
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	RSVD	RSVD	RSVD	RSVD	START DLY	RSVD	RSVD	RSVD

This register provides the ability to over-ride some automatic features of the device.

Bit 7:4 Reserved. Must be zero

Bit 6 Crystal Startup Delay. Setting this bit, sets the crystal startup delay to 150uSec to handle warm restarts of the crystal. Firmware MUST set this bit during initialization.

Bits 2:0 Reserved. Must be zero.

Mnemonic	CLK_OVERRIDE_ADR			Address				0x27
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD

This register provides the ability to over-ride some automatic features of the device.

Bits 7:2 Reserved. Must be zero

Bit 1 Force Receive Clock. Streaming applications MUST set this bit during receive mode, otherwise this bit is cleared.

Bit 0 Reserved. Must be zero.

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Mnemonic	CLK_EN_ADR			Address				0x28
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD

This register provides the ability to over-ride some automatic features of the device.

Bits 7:2 Reserved. Must be zero

Bit 1 Force Receive Clock Enable. Streaming applications MUST set this bit during initialization.

Bit 0 Reserved. Must be zero.

Mnemonic	RX_ABORT_ADR			Address				0x29
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	RSVD	RSVD	ABORT EN	RSVD	RSVD	RSVD	RSVD	RSVD

This register provides the ability to over-ride some automatic features of the device.

Bits 7:6 Reserved. Must be zero

Bit 5 Receive Abort Enable. Typical applications will disrupt any pending receive by first setting this bit, otherwise this bit is cleared.

Bit 4:0 Reserved. Must be zero.

Mnemonic	AUTO_CAL_TIME_ADR			Address				0x32
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	1	1
Read/Write	W	W	W	W	W	W	W	W
Function	AUTO_CAL_TIME							

This register provides the ability to over-ride some automatic features of the device.

Bits 7:6 Auto Cal Time. Firmware MUST write 3Ch to this register during initialization.

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Mnemonic	AUTO_CAL_OFFSET_ADR			Address				0x35
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	AUTO_CAL_OFFSET							

This register provides the ability to over-ride some automatic features of the device.

Bits 7:0 Auto Cal Offset. Firmware MUST write 14h to this register during initialization.

Mnemonic	ANALOG_CTRL_ADR			Address				0x39
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RX INV	ALL SLOW

This register provides the ability to over-ride some automatic features of the device.

Bits 7:2 Reserved. Must be zero

Bit 1 Receive Invert. When set, the incoming receive data is inverted. Firmware MUST set this bit when interoperability with JUNO (CYUSB6934/35)
is desired.

Bit 0 All Slow. When set, the synth setting time for all channels is the same as for slow channels. It is recommended that the firmware set this bit When using GFSK data mode.

Register Files

Files are written to or read from using non-incrementing burst read or write transactions. In most cases accessing a file may be destructive; the file must be completely read/written, otherwise the contents may be altered. When accessing file registers, the bytes are presented to the bus least significant byte first.

Mnemonic	TX_BUFFER_ADR	Address	0x20
Length	16 Bytes	R/W	W
Default	0xXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX		

The transmit buffer is a FIFO. Writing to this file adds a byte to the packet being sent. Writing more bytes to this file than the packet length in TX_LENGTH_ADR will have no effect, and these bytes will be lost. The FIFO accumulates data until it is reset via TX CLR in TX_CTRL_ADR. A previously sent packet, of 16 bytes or less, can be transmitted if TX_GO is set without resetting the FIFO. The contents of TX_BUFFER_ADR is not affected by the transmission of an Auto ACK.

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Mnemonic	RX_BUFFER_ADR	Address	0x21
Length	16 Bytes	R/W	R
Default	0xXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX		

The receive buffer is a FIFO. Received bytes may be read from this file register at any time that it is not empty, but when reading from this file register before a packet has been completely received care must be taken to ensure that error packets (for example with bad CRC16) are handled correctly.
When the receive buffer is configured to be overwritten by new packets (the alternative is for new packets to be discarded if the receive buffer is not empty), similar care must be taken to verify after the packet has been read from the buffer that no part of it was overwritten by a newly received packet while this file register is being read.
When the VLD EN bit in RX_CFG_ADR is set, the bytes in this file register alternate—the first byte read is data, the second byte is a valid flag for each bit in the first byte, the third byte is data, the fourth byte valid flags, etc. In SDR and DDR modes the valid flag for a bit is set if the correlation coefficient for the bit exceeded the correlator threshold, and is cleared if it did not. In 8DR mode, the MSB of a valid flags byte indicates whether or not the correlation coefficient of the corresponding received symbol exceeded the threshold. The seven LSBs contain the number of erroneous chips received for the data.

Mnemonic	SOP_CODE_ADR	Address	0x22
Length	8 Bytes	R/W	R/W
Default	0x17FF9E213690C782		

When using 32 chip SOP_CODE_ADR codes, only the first four bytes of this register are used; in order to complete the file write process, these four bytes must be followed by four bytes of “dummy” data. However, a class of codes known as “multiplicative codes” may be used; there are 64 chip codes with good auto-correlation and cross-correlation properties where the least significant 32 chips themselves have good autocorrelation and cross-correlation properties when used as 32-chip codes. In this case the same eight-byte value may be loaded into this file and used for both 32 chip and 64 chip SOP symbols.
When reading this file, all eight bytes must be read; if fewer than eight bytes are read from the file, the contents of the file will have been rotated by the number of bytes read. This applies to writes, as well.
Recommended SOP Codes:
0x91CCF8E291CC373C
0x0FA239AD0FA1C59B
0x2AB18FD22AB064EF
0x507C26DD507CCD66
0x44F616AD44F6E15C
0x46AE31B646AECC5A
0x3CDC829E3CDC78A1
0x7418656F74198EB9
0x49C1DF6249C0B1DF
0x72141A7F7214E597

Mnemonic	DATA_CODE_ADR	Address	0x23
Length	16 Bytes	R/W	R/W
Default	0x02F9939702FA5CE3012BF1DB0132BE6F		

In GFSK mode, this file register is ignored.

In 64-SDR mode, only the first eight bytes are used.

In 32-DDR mode, only eight bytes are used. The format for these eight bytes: 0x00000000BBBBBBBB00000000AAAAAAAA, where “0” represents unused locations. Example: 0x00000000B2BB092B00000000B86BC0DC; where “B86BC0DC” represents AAAAAAAA, “00000000“ represents unused locations, “B2BB092B“ represents BBBBBBBB, and “00000000“ represents unused locations.

In 64-DDR and 8DR modes, all sixteen bytes are used.

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When reading this file, all sixteen bytes must be read; if fewer than sixteen bytes are read from the file, the contents of the file will have been rotated by the number of bytes read. This applies to writes, as well.

Certain sixteen-byte sequences have been calculated that provide excellent auto-correlation and cross-correlation properties, and it is recommended that such sequences be used; the default value of this register is one such sequence. In typical applications, all devices use the same DATA_CODE_ADR codes, and devices and systems are addressed by using different SOP_CODE_ADR codes; in such cases it may never be necessary to change the contents of this register from the default value.

Typical applications should use the default code.

Mnemonic	PREAMBLE_ADR	Address	0x24
Length	3 Bytes	R/W	R/W
Default	0x333302		

1st byte – The number of repetitions of the preamble sequence that are to be transmitted. The preamble may be disabled by writing 0x00 to this byte.

2nd byte – Least significant eight chips of the preamble sequence

3rd byte – Most significant eight chips of the preamble sequence

If using 64-SDR to communicate with CYWUSB69xx devices, set number of repetitions to four for optimum performance
When reading this file, all three bytes must be read; if fewer than three bytes are read from the file, the contents of the file will have been rotated by the number of bytes read. This applies to writes, as well.

Mnemonic	MFG_ID_ADR	Address	0x25
Length	6 Bytes	R	R
Default	N/A		

To minimize ~190μA of current consumption (default), execute a “dummy” single-byte SPI write to this address with a zero data stage after the contents have been read. Non-zero to enable reading of fuses. Zero to disable reading fuses.

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AC Characteristics

SPI Interface

Parameter	Description	Min	Typ.	Max.	Unit
^{t}SCK_CYC	SPI Clock Period	238.1			ns
^{t}SCK_HI	SPI Clock High Time	100			ns
^{t}SCK_LO	SPI Clock Low Time	100			ns
^{t}DAT_SU	SPI Input Data Set-up Time	25			ns
^{t}DAT_HLD	SPI Input Data Hold Time	10			ns
^{t}DAT_VAL	SPI Output Data Valid Time	0		50	ns
^{t}DAT_VAL_TRI	SPI Output Data Tri-state (MOSI from Slave Select Deassert)			20	ns
^{t}SS_SU	SPI Slave Select Set-up Time before first positive edge of SCK[14]	10			ns
^{t}SS_HLD	SPI Slave Select Hold Time after last negative edge of SCK	10			ns
^{t}SS_PW	SPI Slave Select Minimum Pulse Width	20			ns
^{t}SCK_SU	SPI Slave Select Set-up Time	10			ns
^{t}SCK_HLD	SPI SCK Hold Time	10			ns
^{t}RESET	Minimum RST pin pulse width	10			ns

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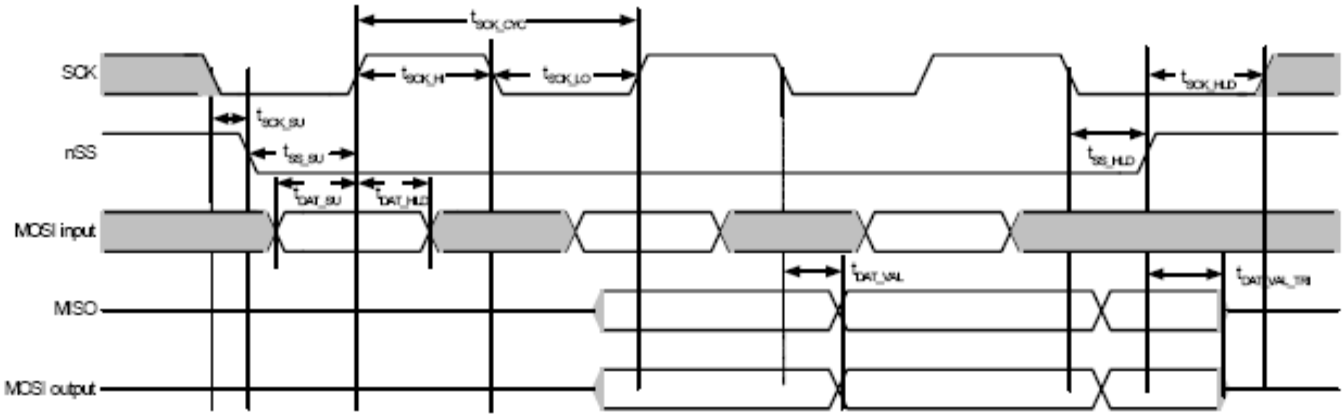
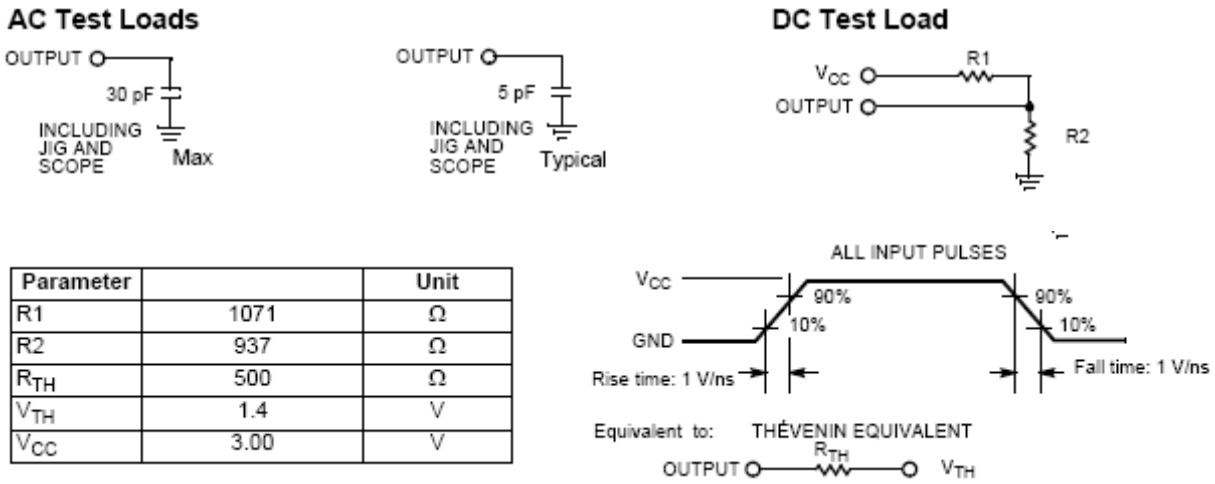
SPI Timing



Notes
12. AC values are not guaranteed if voltage on any pin exceed VIO.
13. CLOAD = 30 pF.
14. SCK must start low at the time SS goes low, otherwise the success of SPI transactions are not guaranteed.

AC Test Loads and Waveforms for Digital Pins



Parameter		Unit
R1	1071	Ω
R2	937	Ω
R_{TH}	500	Ω
V_{TH}	1.4	V
V_{CC}	3.00	V

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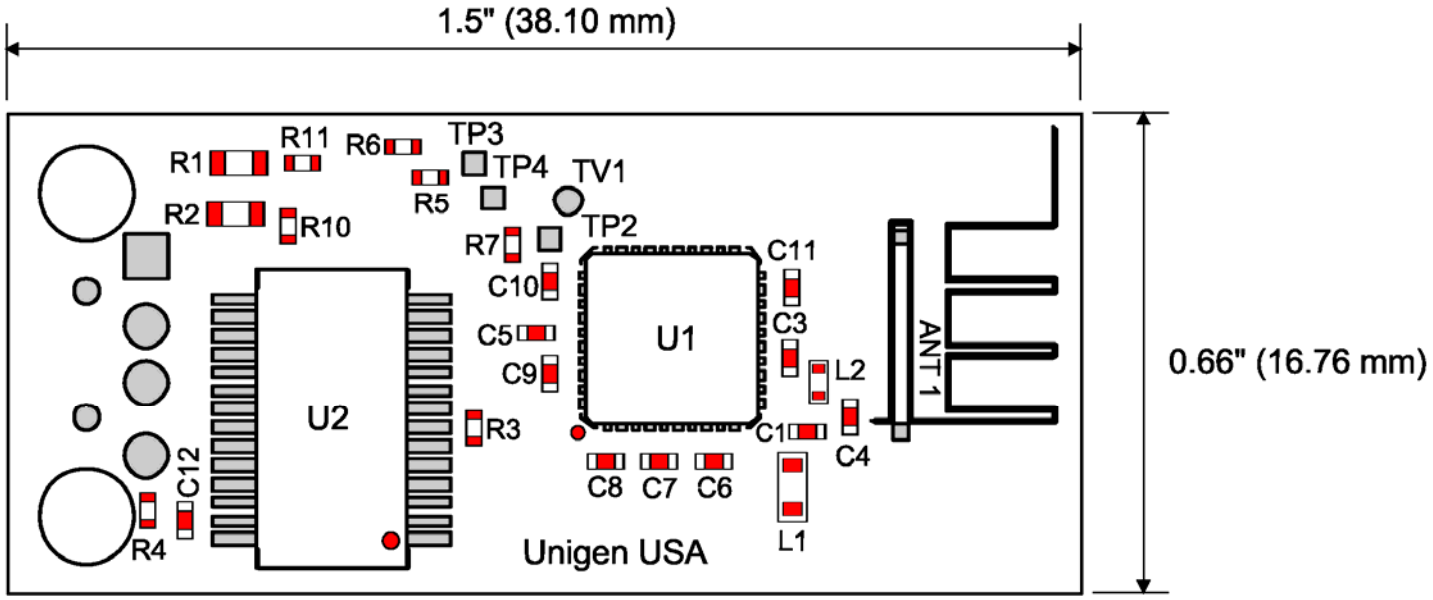
MECHANICAL CHARACTERISTICS:

Item	Description	Specification
1	PCB Material	FR-4
2	PCB Layers	4
3	Connector Type	USB
4	PCB Number	1
5	Flammability Rating	UL94 V-0
6	UGQLUE4US Dimensions	1.5" x 0.66" x 0.224" (38.1mm x 16.8mm x 5.7 mm*) *board to board height
8	Antenna Cable Connector	N/A
9	User Serviceable Parts	None

MECHANICAL DRAWINGS:

Physical Dimensions:



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ORDERING INFORMATION:*

Typical Applications

Unigen Product Group – Wireless -	Form Factor	Process Tech	WirelessUSB Tech			Voltage	Antenna
UGQ	**LU**	**E**	**4US (CYRF6936)**			**50**=5.0Vdc	**Blank**=Mini Coaxial **A=** Integ Antenna

***Module based on the Cypress Semiconductor CYRF6936-48 WirelessUSB™ LP 2.4GHz DSSS Radio SoC device.**

Contact your Unigen Sales Representative for additional information or visit the Nexus™ Wireless Products section of our web site (www.unigen.com).

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Web:	**www.unigen.com**
Customer Comment:	**1.800.826.0808**

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enCoRe™ III Full Speed USB Controller

1.0 Features

- Powerful Harvard Architecture Processor
  - M8C Processor Speeds to 24 MHz
  - Two 8x8 Multiply, 32-bit Accumulate
  - 3.0 to 5.25V Operating Voltage
  - USB Temperature Range: 0°C to +70°C
- Advanced Peripherals (enCoRe™ III Blocks)
  - Analog enCoRe III Block Provides:
    - Up to 14-bit ADCs
  - 4 Digital enCoRe III Blocks Provide:
    - 8-bit PWMs
    - Full-Duplex UART
    - Multiple SPI Masters or Slaves
    - Connectable to all GPIO Pins
- Complex Peripherals by Combining Blocks
- Full-Speed USB (12 Mbps)
  - Four Unidirectional Endpoints
  - One Bidirectional Control Endpoint
  - USB 2.0 Compliant
  - Dedicated 256 Byte Buffer
  - No External Crystal Required
- Flexible On-Chip Memory
  - 16K Flash Program Storage 50,000 Erase/Write Cycles
  - 1K SRAM Data Storage
  - In-System Serial Programming (ISSP)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Programmable Pin Configurations
  - 25-mA Sink on all GPIO
  - Pull-up, Pull-down, High- Z, Strong, or Open Drain Drive Modes on all GPIO
  - Configurable Interrupt on all GPIO
- Precision, Programmable Clocking
  - Internal ±4% 24-/48-MHz Oscillator
  - Internal Oscillator for Watchdog and Sleep
  - 0.25% Accuracy for USB with no External Components
- Additional System Resources
  - I^2C™ Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- Complete Development Tools
  - Free Development Software (PSoC™ Designer)
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Bytes Trace Memory

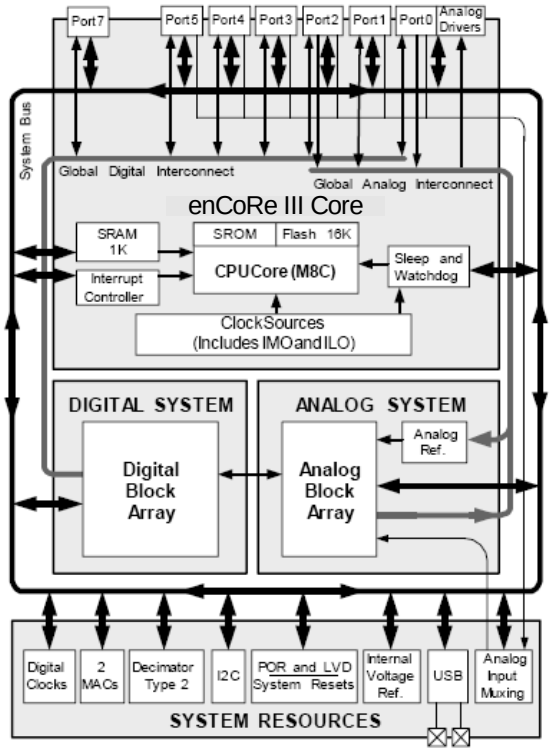


Figure 1-1. enCoRe III Block Diagram

2.0 Applications

- PC HID devices
  - Mice (Optomechanical, Optical, Trackball)
  - Keyboards
  - Joysticks
- Gaming
  - Game Pads
  - Console Keyboards
- General Purpose
  - Barcode Scanners
  - POS Terminal
  - Consumer Electronics
  - Toys
  - Remote Controls
  - USB to Serial

3.0 enCoRe III Functional Overview

enCoRe III is based on the flexible PSoC architecture and is a full-featured, full-speed (12 Mbps) USB part. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of consumer, and communication applications.

This architecture allows the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in both 28-pin SSOP and 56-pin QFN packages.

The enCoRe III architecture, as illustrated in *Figure 1-1*, is comprised of four main areas: enCoRe III Core, Digital System, Analog System, and System Resources including a full-speed USB port. Configurable global busing allows all the device resources to be combined into a complete custom system. The enCoRe III CY7C64215 can have up to seven IO ports that connect to the global digital and analog interconnects, providing access to 4 digital blocks and 1 analog block.

3.1 enCoRe III Core

The enCoRe III Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU utilizes an interrupt controller with up to 20 vectors, to simplify programming of real-time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16K of Flash for program storage, 1K of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

enCoRe III incorporates flexible internal clock generators, including a 24-MHz IMO (internal main oscillator) accurate to 8% over temperature and voltage. The 24-MHz IMO can also be doubled to 48 MHz for use by the digital system. A low-power 32 kHz ILO (internal low-speed oscillator) is provided for the Sleep timer and WDT. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the enCoRe III. In USB systems, the IMO will self-tune to ±0.25% accuracy for USB communication.

enCoRe III GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

3.2 The Digital System

The Digital System is composed of 4 digital enCoRe III blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

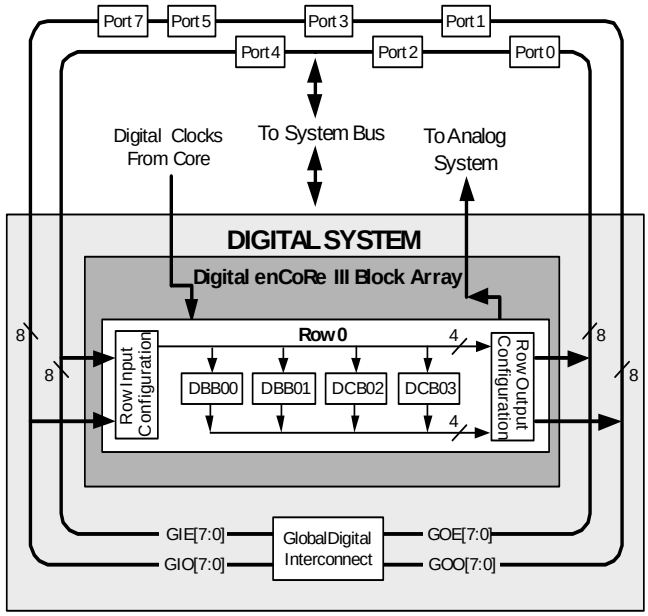


Figure 3-1. Digital System Block Diagram

Digital peripheral configurations include those listed below.

- Full-Speed USB (12 Mbps)
- PWMs (8-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I2C slave and multi-master

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

3.3 The Analog System

The Analog System is composed of 1 configurable block, comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very

flexible and can be customized to support specific application requirements. enCoRe III analog function supports the Analog-to-digital converters (up to 2, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)

Analog blocks are arranged in a column of three, which includes one CT (Continuous Time - AC B00 or AC B01) and two SC (Switched Capacitor - ASC10 and ASD20 or ASD11 and ASC21) blocks, as shown in *Figure 3-2*.

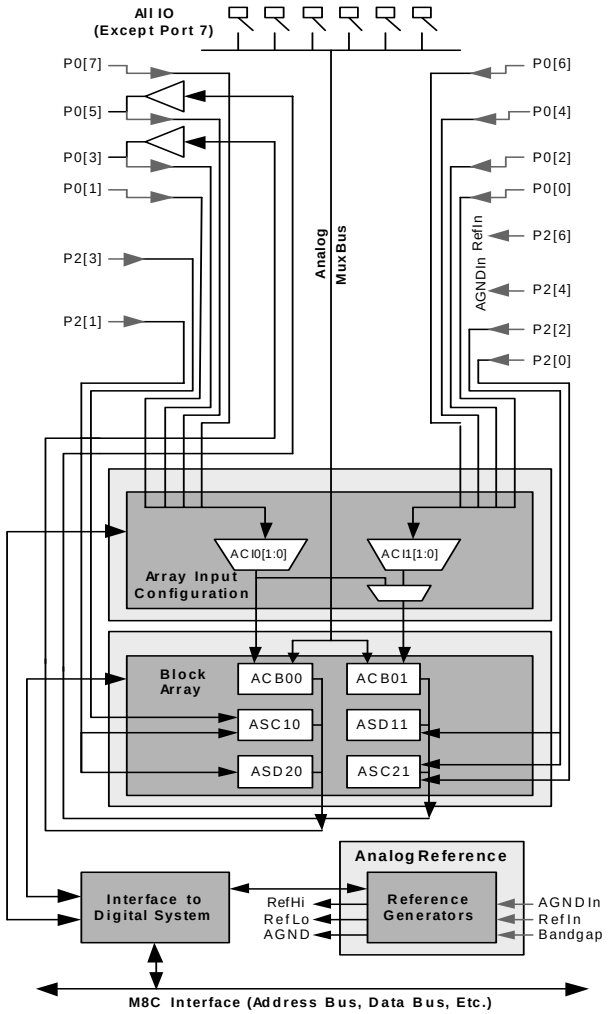


Figure 3-2. Analog System Block Diagram

3.3.1 The Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin in ports 0–5. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

3.4 Additional System Resources

System Resources provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power-on reset. Brief statements describing the merits of each resource follow.

- Full-Speed USB (12 Mbps) with 5 configurable endpoints and 256 bytes of RAM. No external components required except two series resistors. Wider than commercial temperature USB operation (–10°C to +85°C).
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- HAPI interface for a 8-bit bus width to accommodate data transfer with an external microcontroller or similar device.

3.5 enCoRe III Device Characteristics

enCoRe III devices have 4 digital blocks and 6 analog blocks. The following table lists the resources available for specific enCoRe III device.

Table 3-1. enCoRe III Device Characteristics

Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY7C64215 -28PVXC	up to 22	1	4	22	2	2	6	1K	16K
CY7C64215 -56LFXC	up to 50	1	4	48	2	2	6	1K	16K

4.0 Getting Started

The quickest path to understanding enCoRe III silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the enCoRe III integrated circuit and presents specific pin, register, and electrical specifications. enCoRe III is based on the architecture of the CY8C24794. For in-depth information, along with detailed programming information, reference the *PSoC™ Mixed-Signal Array Technical Reference Manual*.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest enCoRe III device data sheets on the web at http://www.cypress.com.

4.1 Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store

contains development kits, **C** compilers, and all accessories for enCoRe III development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *USB (Universal Serial Bus)* to view a current list of available items.

5.0 Development Tools

PSoC Designer is a Microsoft® Windows®-based, integrated development environment for the enCoRe III. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Refer to the PSoC Designer Functional Flow diagram below.)

PSoC Designer helps the customer to select an operating configuration for the enCoRe III, write application code that uses the enCoRe III, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.

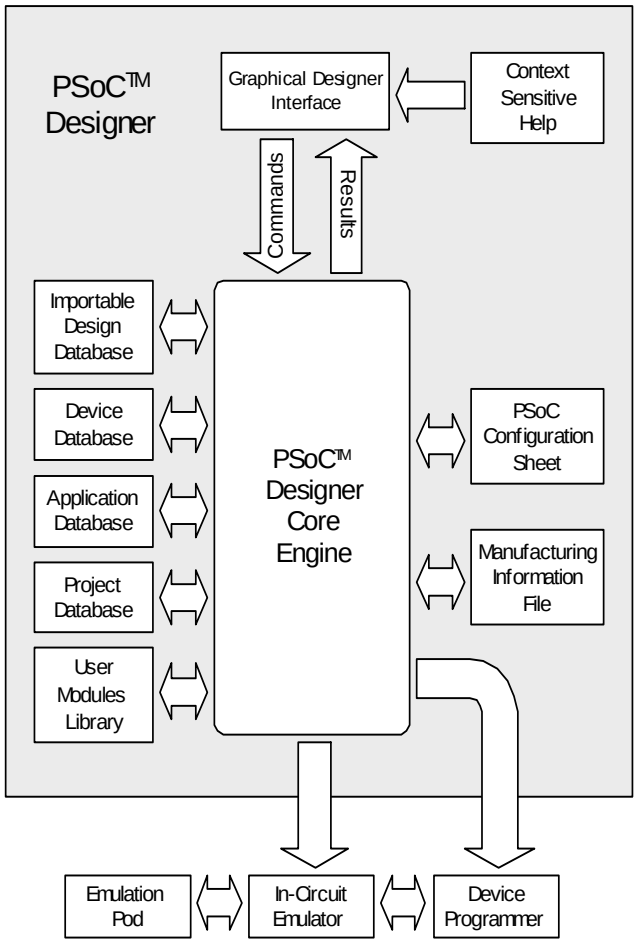


Figure 5-1. PSoC Designer Subsystems

5.1 PSoC Designer Software Subsystems

5.1.1 Device Editor

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the enCoRe III blocks. Examples of user modules are ADCs, SPIM, UART, and PWMs.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected enCoRe III block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of enCoRe III block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

5.1.2 Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports the enCoRe III family of devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the enCoRe III devices.

The embedded, optimizing C compiler provides all the features of C tailored to the enCoRe III architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

5.1.3 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the enCoRe III device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

5.1.4 Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference,

each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

5.2 Hardware Tools

5.2.1 In-Circuit Emulator

A low-cost, high-functionality ICE Cube is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and will operate with all enCoRe III devices.

6.0 Designing with User Modules

The development process for the enCoRe III device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the enCoRe III architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called enCoRe III Blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses and to the IO pins. Iterative development cycles permit you to adapt the hardware as well as the software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of pre-built, pre-tested hardware peripheral functions, called “User Modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties. The User Module library contains 8 peripherals: ADCINC, PWM8, UART, SPIM, SPIS, LCD, I2CHW, I2CM and USBFS.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit the designer to establish the pulse width and duty cycle. User modules also provide tested software to cut development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run-time. The API also provides optional interrupt service routines that can be adapted as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a graphical user interface (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by interconnecting user modules to each other and the IO pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.

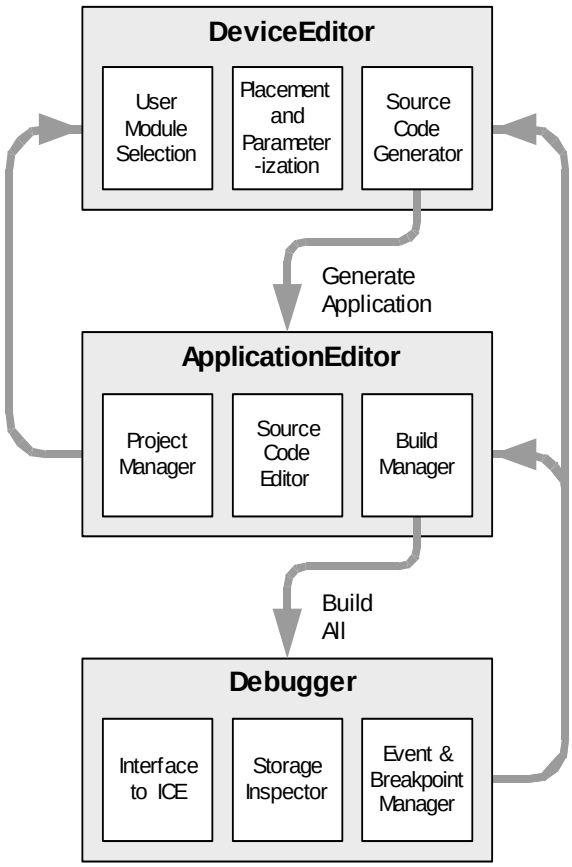


Figure 6-1. User Module and Source Code Development Flows

The next step is to write your main program, and any subroutines using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager. It employs a professional-strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE CUBE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

7.0 Document Conventions

7.1 Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SRAM	static random access memory

7.2 Units of Measure

A units of measure table is located in the Electrical Specifications section. *Table 11-1* on page 11 lists all the abbreviations used to measure the enCoRe III devices.

7.3 Numeric Naming

Hexidecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexidecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (e.g., 01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

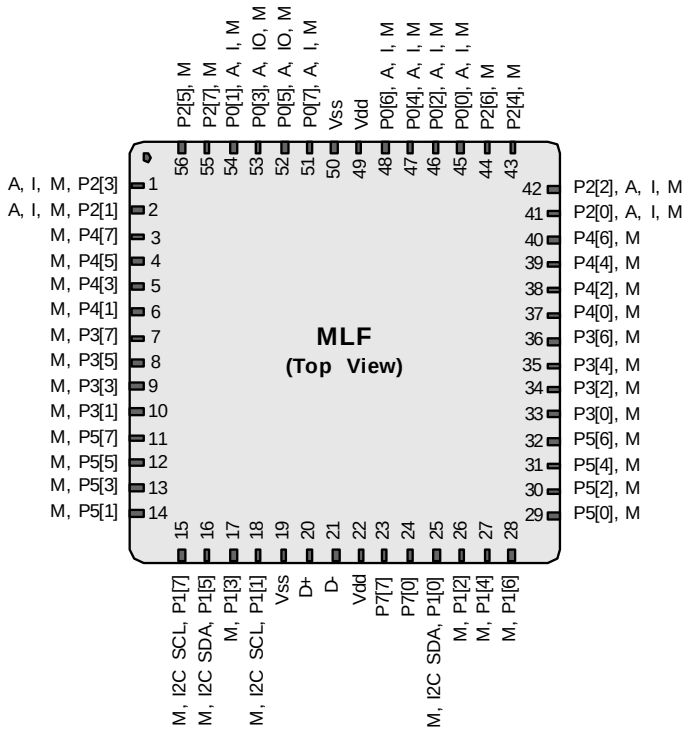
8.0 56-Pin Part Pinout

The CY7C64215 enCoRe III device is available in a 56-pin package which is listed and illustrated in the following table. Every port pin (labeled with a “P”) is capable of Digital IO. However, Vss and Vdd are not capable of Digital IO.

Table 8-1. 56-Pin Part Pinout (MLF*)

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I, M	P2[3]	Direct switched capacitor block input.
2	IO	I, M	P2[1]	Direct switched capacitor block input.
3	IO	M	P4[7]	
4	IO	M	P4[5]	
5	IO	M	P4[3]	
6	IO	M	P4[1]	
7	IO	M	P3[7]	
8	IO	M	P3[5]	
9	IO	M	P3[3]	
10	IO	M	P3[1]	
11	IO	M	P5[7]	
12	IO	M	P5[5]	
13	IO	M	P5[3]	
14	IO	M	P5[1]	
15	IO	M	P1[7]	I2C Serial Clock (SCL).
16	IO	M	P1[5]	I2C Serial Data (SDA).
17	IO	M	P1[3]	
18	IO	M	P1[1]	I2C Serial Clock (SCL), ISSP-SCLK.
19	Power		Vss	Ground connection.
20	USB		D+	
21	USB		D-	
22	Power		Vdd	Supply voltage.
23	IO		P7[7]	
24	IO		P7[0]	
25	IO	M	P1[0]	I2C Serial Data (SDA), ISSP-SDATA.
26	IO	M	P1[2]	
27	IO	M	P1[4]	
28	IO	M	P1[6]	
29	IO	M	P5[0]	
30	IO	M	P5[2]	
31	IO	M	P5[4]	
32	IO	M	P5[6]	
33	IO	M	P3[0]	
34	IO	M	P3[2]	
35	IO	M	P3[4]	
36	IO	M	P3[6]	
37	IO	M	P4[0]	
38	IO	M	P4[2]	
39	IO	M	P4[4]	
40	IO	M	P4[6]	
41	IO	I, M	P2[0]	Direct switched capacitor block input.
42	IO	I, M	P2[2]	Direct switched capacitor block input.
43	IO	M	P2[4]	External Analog Ground (AGND) input.
44	IO	M	P2[6]	External Voltage Reference (VREF) input.
45	IO	I, M	P0[0]	Analog column mux input.
46	IO	I, M	P0[2]	Analog column mux input and column output.
47	IO	I, M	P0[4]	Analog column mux input and column output.
48	IO	I, M	P0[6]	Analog column mux input.
49	Power		Vdd	Supply voltage.
50	Power		Vss	Ground connection.
51	IO	I, M	P0[7]	Analog column mux input, integration input #1.
52	IO	IO, M	P0[5]	Analog column mux input and column output, integration input #2.
53	IO	IO, M	P0[3]	Analog column mux input and column output.
54	IO	I, M	P0[1]	Analog column mux input.
55	IO	M	P2[7]	
56	IO	M	P2[5]	

CY7C64215 56-Pin enCoRe III Device



LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.
* The MLF package has a center pad that must be connected to ground (Vss).

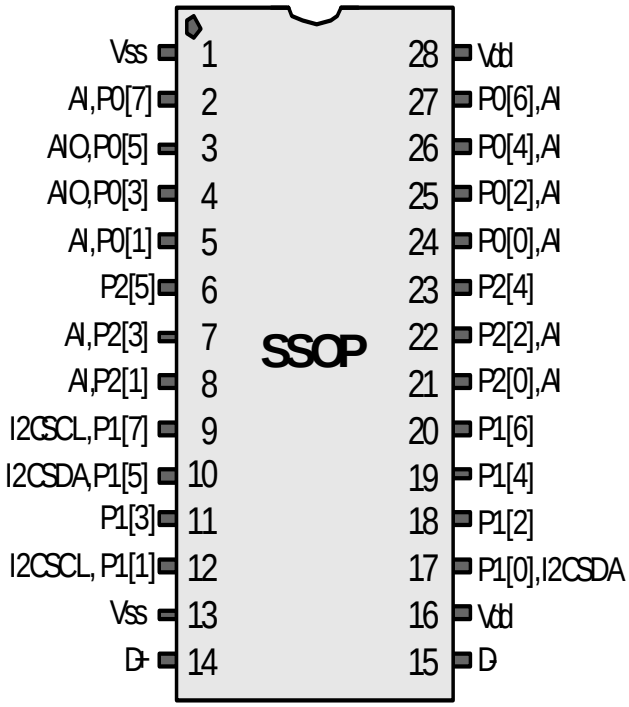
9.0 28-Pin Part Pinout

The CY7C64215 enCoRe III device is available in a 28-pin package which is listed and illustrated in the following table. Every port pin (labeled with a “P”) is capable of Digital IO. However, Vss and Vdd are not capable of Digital IO.

Table 9-1. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Name	Description
	Digital	Analog		
1	Power		GND	Ground connection
2	IO	I, M	P0[7]	Analog column mux input, integration input #1.
3	IO	IO,M	P0[5]	Analog column mux input and column output, integration input #2.
4	IO	IO,M	P0[3]	Analog column mux input and column output.
5	IO	I,M	P0[1]	Analog column mux input.
6	IO	M	P2[5]	
7	IO	M	P2[3]	Direct switched capacitor block input.
8	IO	M	P2[1]	Direct switched capacitor block input.
9	IO	M	P1[7]	I2C Serial Clock (SCL).
10	IO	M	P1[5]	I2C Serial Data (SDA).
11	IO	M	P1[3]	
12	IO	M	P1[1]	I2C Serial Clock (SCL), ISSP-SCLK.
13	Power		GND	Ground connection
14	USB		D+	
15	USB		D-]	
16	Power		Vdd	Supply voltage.
17	IO	M	P1[0]	I2C Serial Data (SDA), ISSP-SDATA.
18	IO	M	P1[2]	
19	IO	M	P1[4]	
20	IO	M	P1[6]	
21	IO	M	P2[0]	Direct switched capacitor block input.
22	IO	M	P2[2]	Direct switched capacitor block input.
23	IO	M	P2[4]	External Analog Ground (AGND) input.
24	IO	M	P0[0]	Analog column mux input.
25	IO	M	P0[2]	Analog column mux input and column output.
26	IO	M	P0[4]	Analog column mux input and column output.
27	IO	M	P0[6]	Analog column mux input.
28	Power		Vdd]	Supply voltage.

CY7C64215 28-Pin enCoRe III Device



LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.
* The MLF package has a center pad that must be connected to ground (Vss).

10.0 Register Reference

10.1 Register Conventions

10.1.1 Abbreviations Used

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

10.2 Register Mapping Tables

The enCoRe III device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

10.3 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	PMA0_DR	40	RW	ASC10CR0	80	RW		C0	
PRT0IE	01	RW	PMA1_DR	41	RW	ASC10CR1	81	RW		C1	
PRT0GS	02	RW	PMA2_DR	42	RW	ASC10CR2	82	RW		C2	
PRT0DM2	03	RW	PMA3_DR	43	RW	ASC10CR3	83	RW		C3	
PRT1DR	04	RW	PMA4_DR	44	RW	ASD11CR0	84	RW		C4	
PRT1IE	05	RW	PMA5_DR	45	RW	ASD11CR1	85	RW		C5	
PRT1GS	06	RW	PMA6_DR	46	RW	ASD11CR2	86	RW		C6	
PRT1DM2	07	RW	PMA7_DR	47	RW	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	USB_SOF0	48	R		88			C8	
PRT2IE	09	RW	USB_SOF1	49	R		89			C9	
PRT2GS	0A	RW	USB_CR0	4A	RW		8A			CA	
PRT2DM2	0B	RW	USBIO_CR0	4B	#		8B			CB	
PRT3DR	0C	RW	USBIO_CR1	4C	RW		8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW	EP1_CNT1	4E	#		8E			CE	
PRT3DM2	0F	RW	EP1_CNT	4F	RW		8F			CF	
PRT4DR	10	RW	EP2_CNT1	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	EP2_CNT	51	RW	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	EP3_CNT1	52	#	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	EP3_CNT	53	RW	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	EP4_CNT1	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	EP4_CNT	55	RW	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	EP0_CR	56	#	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	EP0_CNT	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
	18		EP0_DR0	58	RW		98		I2C_DR	D8	RW
	19		EP0_DR1	59	RW		99		I2C_MSCR	D9	#
	1A		EP0_DR2	5A	RW		9A		INT_CLR0	DA	RW
	1B		EP0_DR3	5B	RW		9B		INT_CLR1	DB	RW
PRT7DR	1C	RW	EP0_DR4	5C	RW		9C		INT_CLR2	DC	RW
PRT7IE	1D	RW	EP0_DR5	5D	RW		9D		INT_CLR3	DD	RW
PRT7GS	1E	RW	EP0_DR6	5E	RW		9E		INT_MSK3	DE	RW
PRT7DM2	1F	RW	EP0_DR7	5F	RW		9F		INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

10.4 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	PMA0_WA	40	RW	ASC10CR0	80	RW	USBIO_CR2	C0	RW
PRT0DM1	01	RW	PMA1_WA	41	RW	ASC10CR1	81	RW	USB_CR1	C1	#
PRT0IC0	02	RW	PMA2_WA	42	RW	ASC10CR2	82	RW			
PRT0IC1	03	RW	PMA3_WA	43	RW	ASC10CR3	83	RW			
PRT1DM0	04	RW	PMA4_WA	44	RW	ASD11CR0	84	RW	EP1_CR0	C4	#
PRT1DM1	05	RW	PMA5_WA	45	RW	ASD11CR1	85	RW	EP2_CR0	C5	#
PRT1IC0	06	RW	PMA6_WA	46	RW	ASD11CR2	86	RW	EP3_CR0	C6	#
PRT1IC1	07	RW	PMA7_WA	47	RW	ASD11CR3	87	RW	EP4_CR0	C7	#
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
PRT4DM0	10	RW	PMA0_RA	50	RW		90		GDI_O_IN	D0	RW
PRT4DM1	11	RW	PMA1_RA	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	PMA2_RA	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW	PMA3_RA	53	RW	ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	PMA4_RA	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	PMA5_RA	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	PMA6_RA	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW	PMA7_RA	57	RW	ASC21CR3	97	RW		D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
PRT7DM0	1C	RW		5C			9C			DC	
PRT7DM1	1D	RW		5D			9D		OSC_GO_EN	DD	RW
PRT7IC0	1E	RW		5E			9E		OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW	CMP_GO_EN1	65	RW		A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC		MUX_CR4	EC	RW
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD		MUX_CR5	ED	RW
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

11.0 Electrical Specifications

This section presents the DC and AC electrical specifications of the CY7C64215 enCoRe III. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com.

Specifications are valid for 0°C ≤ T_A ≤ 70°C and T_J ≤ 100°C, except where noted. Specifications for devices running at greater than 12 MHz are valid for 0°C ≤ T_A ≤ 70°C and T_J ≤ 82°C.

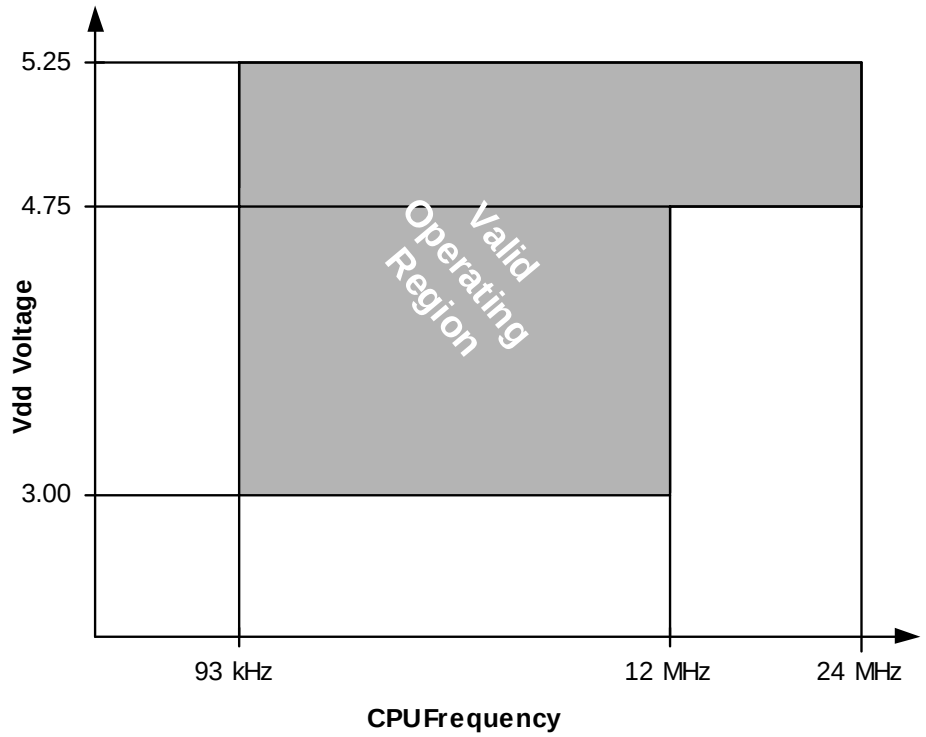


Figure 11-1. Voltage versus CPU Frequency

The following table lists the units of measure that are used in this section.

Table 11-1. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milliampere
fF	femto farad	ms	millisecond
Hz	hertz	mV	millivolts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	W	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	s	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

11.1 Absolute Maximum Ratings

Table 11-2. Absolute Maximum Ratings

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{STG}	Storage Temperature	–55	–	+100	°C	Higher storage temperatures will reduce data retention time.
T_A	Ambient Temperature with Power Applied	–40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	–0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss – 0.5	–	Vdd + 0.5	V	
V_{IO2}	DC Voltage Applied to Tri-state	Vss – 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	–25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	–50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

11.2 Operating Temperature

Table 11-3. Operating Temperature

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_A	Ambient Temperature	0	–	+70	°C	
T_J	Junction Temperature	0	–	+88	°C	The temperature rise from ambient to junction is package specific. See “Thermal Impedance” on page 24. The user must limit the power consumption to comply with this requirement.

11.3 DC Electrical Characteristics

11.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-4. DC Chip-Level Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
Vdd	Supply Voltage	3.0	–	5.25	V	See DC POR and LVD specifications, *Table 11-12* on page 16.
I_{DD5}	Supply Current, IMO = 24 MHz (5V)	–	14	27	mA	Conditions are Vdd = 5.0V, T_A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{DD3}	Supply Current, IMO = 24 MHz (3.3V)	–	8	14	mA	Conditions are Vdd = 3.3V, T_A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[1]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 0°C ≤ T_A ≤ 55°C, analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[1]	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55°C < T_A ≤ 70°C, analog power = off.

Note:
1. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

11.3.2 DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-5. DC GPIO Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
R_{PU}	Pull-Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull-Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd – 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined IOL budget.
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25.
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25.
V_H	Input Hysteresis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

11.3.3 DC Full-Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-6. DC Full-Speed (12 Mbps) USB Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
USB Interface						
V_{DI}	Differential Input Sensitivity	0.2	–	–	V	| (D+) – (D–) |
V_{CM}	Differential Input Common Mode Range	0.8	–	2.5	V	
V_{SE}	Single Ended Receiver Threshold	0.8	–	2.0	V	
C_{IN}	Transceiver Capacitance	–	–	20	pF	
I_{IO}	High-Z State Data Line Leakage	–10	–	10	µA	0V < V_{IN} < 3.3V.
R_{EXT}	External USB Series Resistor	23	–	25	W	In series with each USB pin.
V_{UOH}	Static Output High, Driven	2.8	–	3.6	V	15 kΩ ± 5% to Ground. Internal pull-up enabled.
V_{UOHI}	Static Output High, Idle	2.7	–	3.6	V	15 kΩ ± 5% to Ground. Internal pull-up enabled.
V_{UOL}	Static Output Low	–	–	0.3	V	15 kΩ ± 5% to Ground. Internal pull-up enabled.
Z_O	USB Driver Output Impedance	28	–	44	W	Including R_{EXT} Resistor.
V_{CRS}	D+/D– Crossover Voltage	1.3	–	2.0	V	

11.3.4 DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-7. 5V DC Analog Output Buffer Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 0.6 0.6	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd – 1.3 0.5 x Vdd – 1.3	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	53	64	–	dB	(0.5 x Vdd – 1.3) ≤ V_{OUT} ≤ (Vdd – 2.3).

Table 11-8. 3.3V DC Analog Output Buffer Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd – 1.0 0.5 x Vdd – 1.0	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	34	64	–	dB	(0.5 x Vdd – 1.0) ≤ V_{OUT} ≤ (0.5 x Vdd + 0.9).

11.3.5 DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-9. 5V DC Analog Reference Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[2]	Vdd/2 – 0.04	Vdd/2 – 0.01	Vdd/2 + 0.007	V
–	AGND = 2 x BandGap[2]	2 x BG – 0.048	2 x BG – 0.030	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)[2]	P2[4] – 0.011	P2[4]	P2[4] + 0.011	V
–	AGND = BandGap[2]	BG – 0.009	BG + 0.008	BG + 0.016	V
–	AGND = 1.6 x BandGap[2]	1.6 x BG – 0.022	1.6 x BG – 0.010	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[2]	–0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + BG – 0.10	Vdd/2 + BG	Vdd/2 + BG + 0.10	V
–	RefHi = 3 x BandGap	3 x BG – 0.06	3 x BG	3 x BG + 0.06	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] – 0.113	2 x BG + P2[6] – 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG – 0.130	P2[4] + BG – 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] – 0.133	P2[4] + P2[6] – 0.016	P2[4] + P2[6]+ 0.100	V
–	RefHi = 3.2 x BandGap	3.2 x BG – 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 – BG – 0.04	Vdd/2 – BG + 0.024	Vdd/2 – BG + 0.04	V
–	RefLo = BandGap	BG – 0.06	BG	BG + 0.06	V
–	RefLo = 2 x BandGap – P2[6] (P2[6] = 1.3V)	2 x BG – P2[6] – 0.084	2 x BG – P2[6] + 0.025	2 x BG – P2[6] + 0.134	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] – BG – 0.056	P2[4] – BG + 0.026	P2[4] – BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] – P2[6] – 0.057	P2[4] – P2[6] + 0.026	P2[4] – P2[6] + 0.110	V

Table 11-10. 3.3V DC Analog Reference Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[2]	Vdd/2 – 0.03	Vdd/2 – 0.01	Vdd/2 + 0.005	V
–	AGND = 2 x BandGap[2]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] – 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap[2]	BG – 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6 x BandGap[2]	1.6 x BG – 0.027	1.6 x BG – 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)[2]	–0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] – 0.075	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap	Not Allowed			
–	RefLo = Vdd/2 – BandGap	Not Allowed			
–	RefLo = BandGap	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] – P2[6] – 0.048	P2[4] – P2[6] + 0.022	P2[4] – P2[6] + 0.092	V

Note:
2. AGND tolerance includes the offsets of the local buffer in the enCoRe III block. Bandgap voltage is 1.3V ± 0.02V.

11.3.6 DC Analog enCoRe III Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-11. DC Analog enCoRe III Block Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

11.3.7 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *PSoC Mixed-Signal Array Technical Reference Manual* for more information on the VLT_CR register.

Table 11-12. DC POR and LVD Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
	Vdd Value for PPOR Trip (positive ramp)					
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V	
	Vdd Value for PPOR Trip (negative ramp)					
V_{PPOR0}	PORLEV[1:0] = 00b		2.82		V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55		V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[3]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[4]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	

Notes:
3. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
4. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

11.3.8 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-13. DC Programming Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDP}	Supply Current During Programming or Verify	–	15	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.1	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd – 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[5]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Note:

5. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

   For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

11.4 AC Electrical Characteristics

11.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-14. AC Chip-Level Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
$F_{IMO245V}$	Internal Main Oscillator Frequency for 24 MHz (5V)	23.04	24	24.96[6, 7]	MHz	Trimmed for 5V operation using factory trim values.
$F_{IMO243V}$	Internal Main Oscillator Frequency for 24 MHz (3.3V)	22.08	24	25.92[6,8]	MHz	Trimmed for 3.3V operation using factory trim values.
F_{IMOUSB}	Internal Main Oscillator Frequency with USB Frequency locking enabled and USB traffic present.	23.94	24	24.06[7]	MHz	0°C ≤ T_A ≤ 70°C
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.96[6,7]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.96[7, 8]	MHz	
F_{BLK5}	Digital PSoC Block Frequency (5V Nominal)	0	48	49.92[6, 7, 9]	MHz	Refer to the AC Digital Block Specifications.
F_{BLK3}	Digital PSoC Block Frequency (3.3V Nominal)	0	24	25.92[7, 9]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
Jitter32k	32-kHz Period Jitter	–	100		ns	
Step24M	24-MHz Trim Step Size	–	50	–	kHz	
Fout48M	48-MHz Output Frequency	46.08	48.0	49.92[6, 8]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24-MHz Period Jitter (IMO) Peak-to-Peak	–	300		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.96	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

Notes:
6. 4.75V < Vdd < 5.25V.
7. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
8. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
9. See the individual user module data sheets for information on maximum frequencies for user modules.

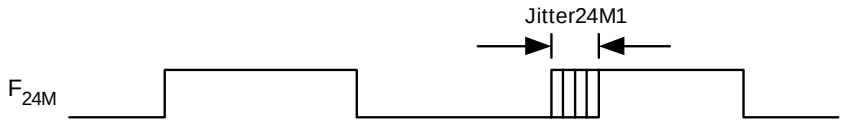


Figure 11-2. 24 MHz Period Jitter (IMO) Timing Diagram

11.4.2 AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-15. AC GPIO Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10%–90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10%–90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10%–90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10%–90%

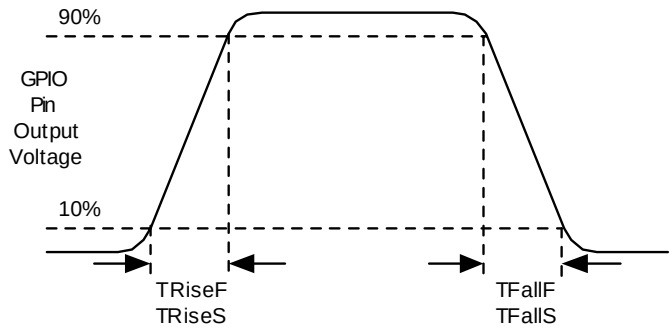


Figure 11-3. GPIO Timing Diagram

11.4.3 AC Full-Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-16. AC Full-Speed (12 Mbps) USB Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{RFS}	Transition Rise Time	4	–	20	ns	For 50 pF load.
T_{FSS}	Transition Fall Time	4	–	20	ns	For 50 pF load.
T_{RFMFS}	Rise/Fall Time Matching: (T_R/T_F)	90	–	111	%	For 50 pF load.
$T_{DRATEFS}$	Full-Speed Data Rate	12 – 0.25%	12	12 + 0.25%	Mbps	

11.4.4 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-17. AC Digital Block Specifications

Function	Description	Min.	Typ.	Max.	Unit	Notes
Timer	Capture Pulse Width	50[10]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	25.92	MHz	
Counter	Enable Pulse Width	50[10]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	25.92	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[10]	–	–	ns	
	Disable Mode	50[10]	–	–	ns	
	Maximum Frequency	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50[10]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.

Note:
10. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

11.4.5 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-18. AC External Clock Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
F_{OSCEXT}	Frequency for USB Applications	23.94	24	24.06	MHz	
–	Duty Cycle	47	50	53	%	
–	Power up to IMO Switch	150	–	–	µs	

11.4.6 AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-19. 5V AC Analog Output Buffer Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100-pF Load					
	Power = Low	–	–	2.5	µs	
	Power = High	–	–	2.5	µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100-pF Load					
	Power = Low	–	–	2.2	µs	
	Power = High	–	–	2.2	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100-pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100-pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
BW_{OBSS}	Small Signal Bandwidth, 20mV_{pp}, 3-dB BW, 100-pF Load					
	Power = Low	0.8	–	–	MHz	
	Power = High	0.8	–	–	MHz	
BW_{OBLS}	Large Signal Bandwidth, 1V_{pp}, 3-dB BW, 100-pF Load					
	Power = Low	300	–	–	kHz	
	Power = High	300	–	–	kHz	

Table 11-20. 3.3V AC Analog Output Buffer Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100-pF Load					
	Power = Low	–	–	3.8	µs	
	Power = High	–	–	3.8	µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100-pF Load					
	Power = Low	–	–	2.6	µs	
	Power = High	–	–	2.6	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100-pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100-pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
BW_{OBSS}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100-pF Load					
	Power = Low	0.7	–	–	MHz	
	Power = High	0.7	–	–	MHz	
BW_{OBLS}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100-pF Load					
	Power = Low	200	–	–	kHz	
	Power = High	200	–	–	kHz	

11.4.7 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-21. AC Programming Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	Vdd > 3.6
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6

11.4.8 AC I^2C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and 0°C ≤ T_A ≤ 70°C, or 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-22. AC Characteristics of the I^2C SDA and SCL Pins for Vdd

Parameter	Description	Standard Mode		Fast Mode		Unit	Notes
		Min.	Max.	Min.	Max.		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[11]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Note:

11. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

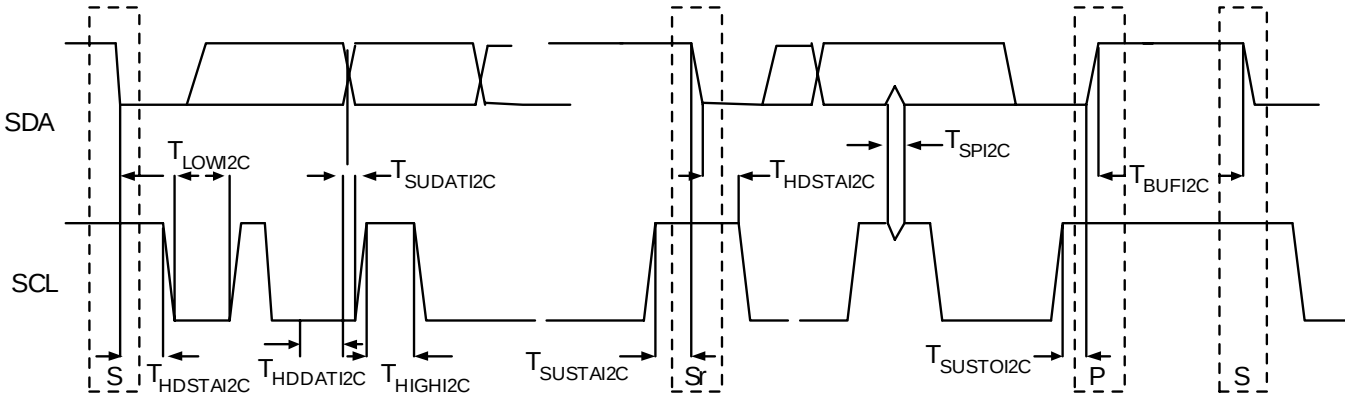


Figure 11-4. Definition for Timing for Fast/Standard Mode on the I²C Bus

12.0 Packaging Information

This section illustrates the package specification for the CY7C64215 enCoRe III, along with the thermal impedance for the package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/support/link.cfm?mr=poddim.

12.1 Packaging Dimensions

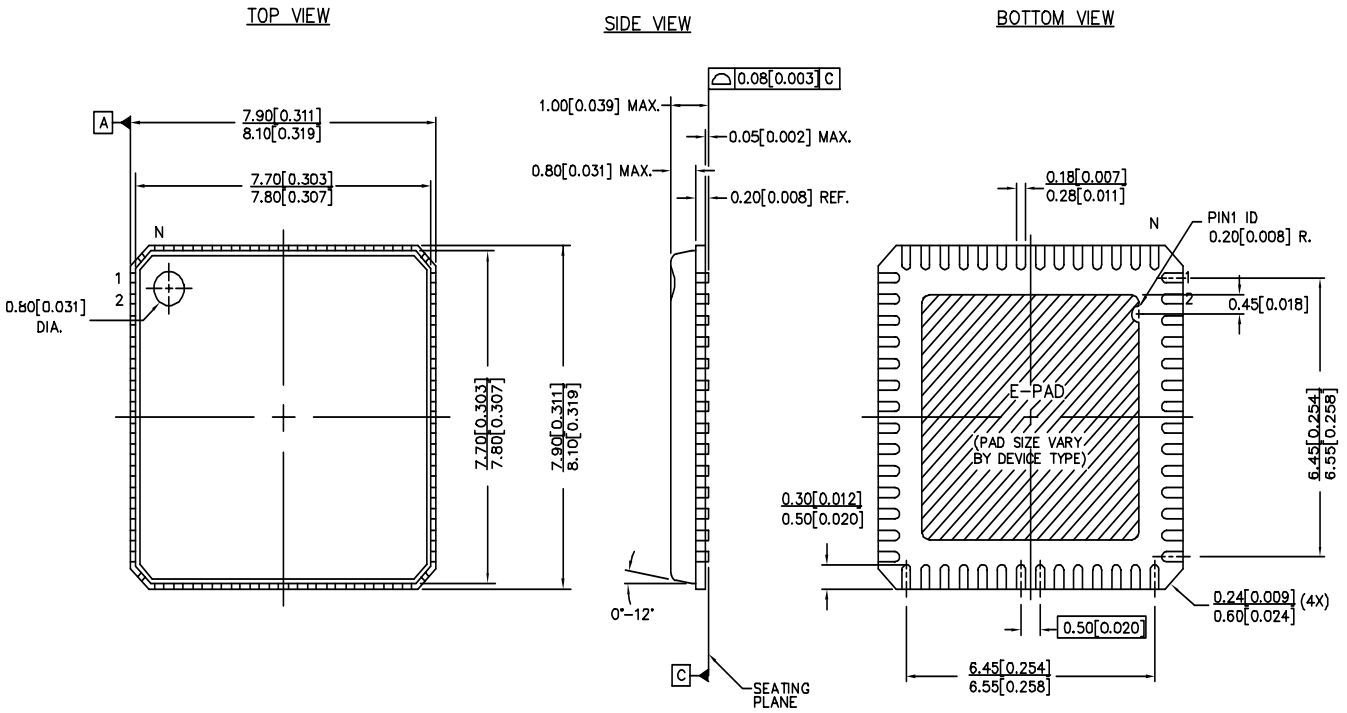


Figure 12-1. 56-Lead (8x8 mm) MLF

Important Note For information on the preferred dimensions for mounting MLF packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

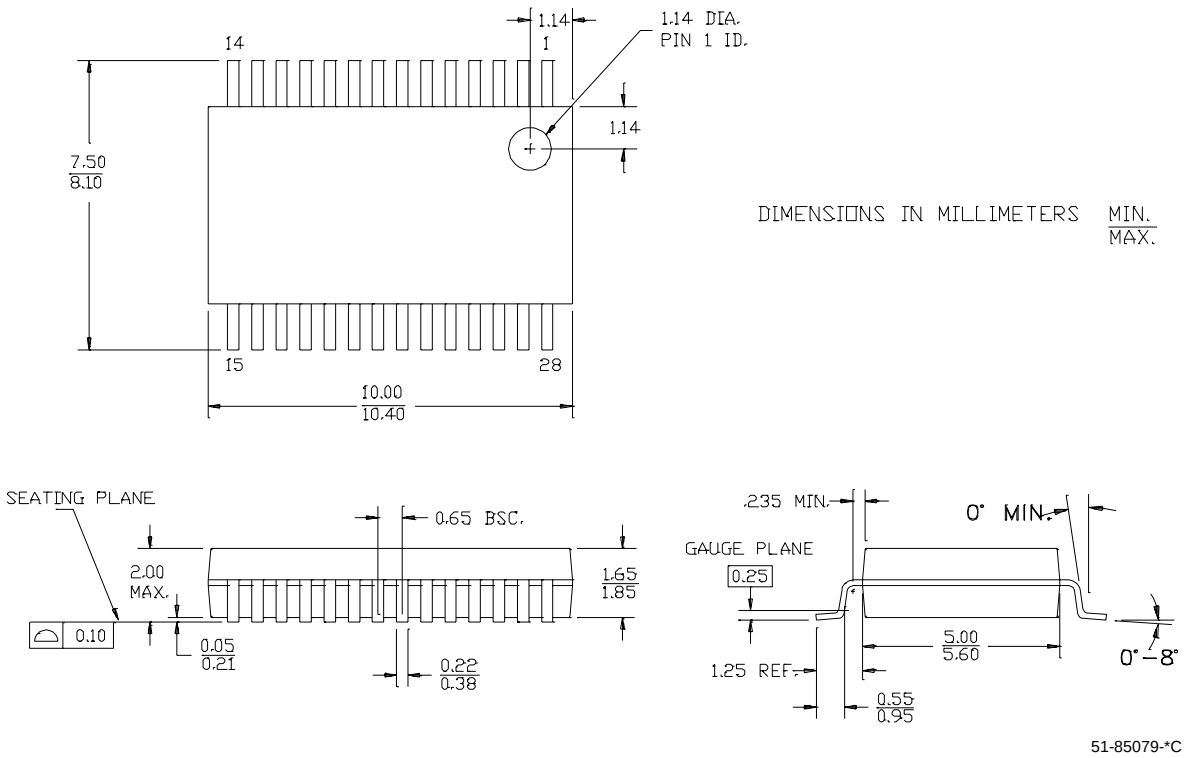


Figure 12-2. 28-Lead Shrunk Small Outline Package

12.2 Thermal Impedance

Table 12-1. Thermal Impedance for the Package

Package	Typical θ_{JA} *
56 MLF	20 °C/W
28 SSOP	96 °C/W

* $T_J = T_A + POWER \times \theta_{JA}$

12.3 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 12-2. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature*	Maximum Peak Temperature
56 MLF	240°C	260°C
28 SSOP	240°C	260°C

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220±5°C with Sn-Pb or 245±5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

13.0 Ordering Information

Table 13-1. CY8C24794 PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash Size	SRAM (Bytes)
56 Pin MLF	CY7C64215-56LFXC	16K	1K
28 Pin SSOP	CY7C64215-28PVXC	16K	1K

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Document History Page

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	131325	See ECN	XGR	New data sheet
*A	385256	See ECN	BHA	Changed from Advance Information to Preliminary. Added standard data sheet items. Changed Part number from CY7C642xx to CY7C64215.